

# Compal confidential

## Schematics Document

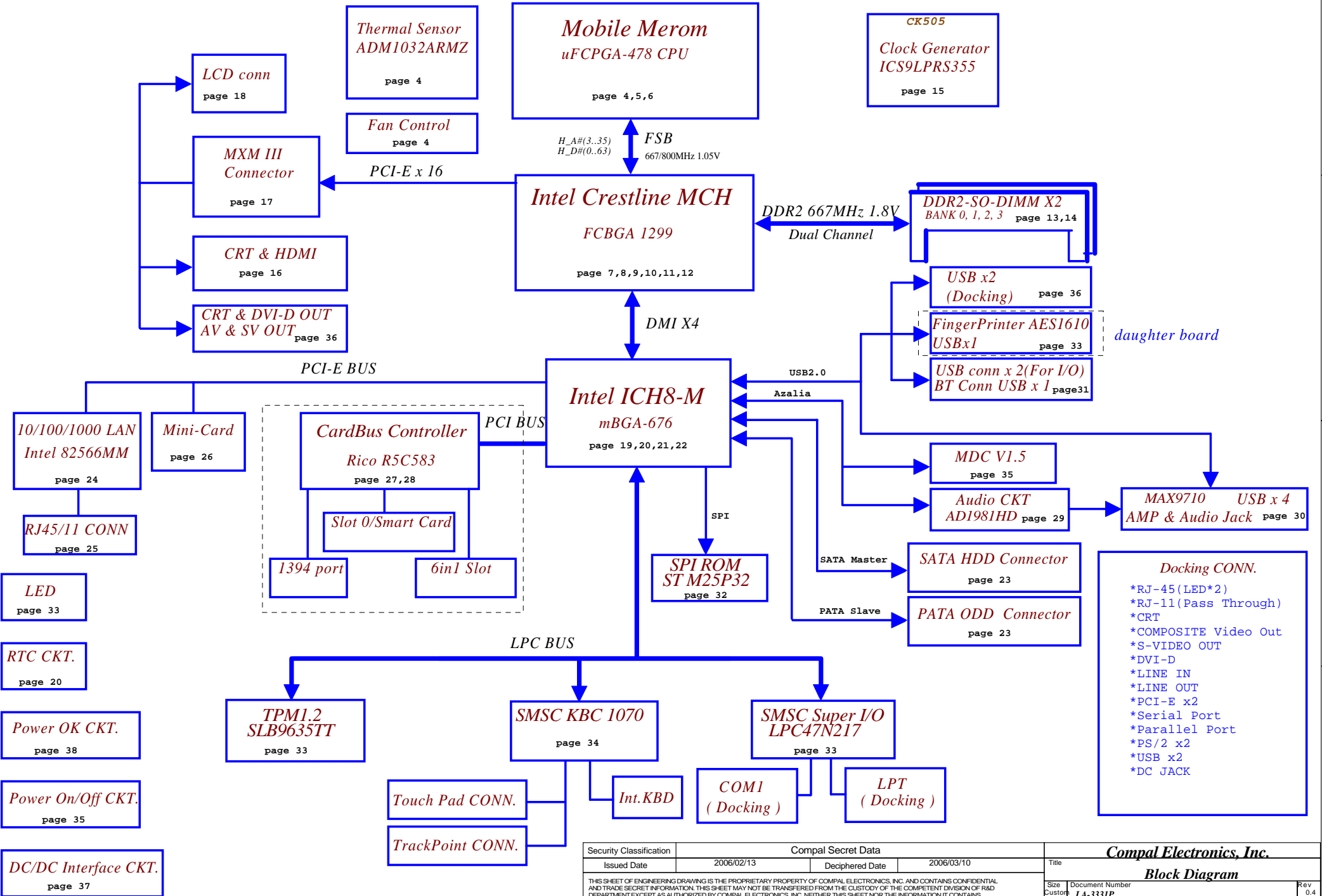
Mobile Merom uFCPGA with Intel  
Crestline\_PM+ICH8-M core logic

2006-11-10

REV:0.4

Security Classification		Compal Secret Data		Title	
Issued Date	2006/04/13	Deciphered Date	2006/06/30	Cover Sheet	
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# ABITA



## Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+3VM +1.25VM +1.05VM	+5V +1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON X MEANS OFF

## PCI Devices

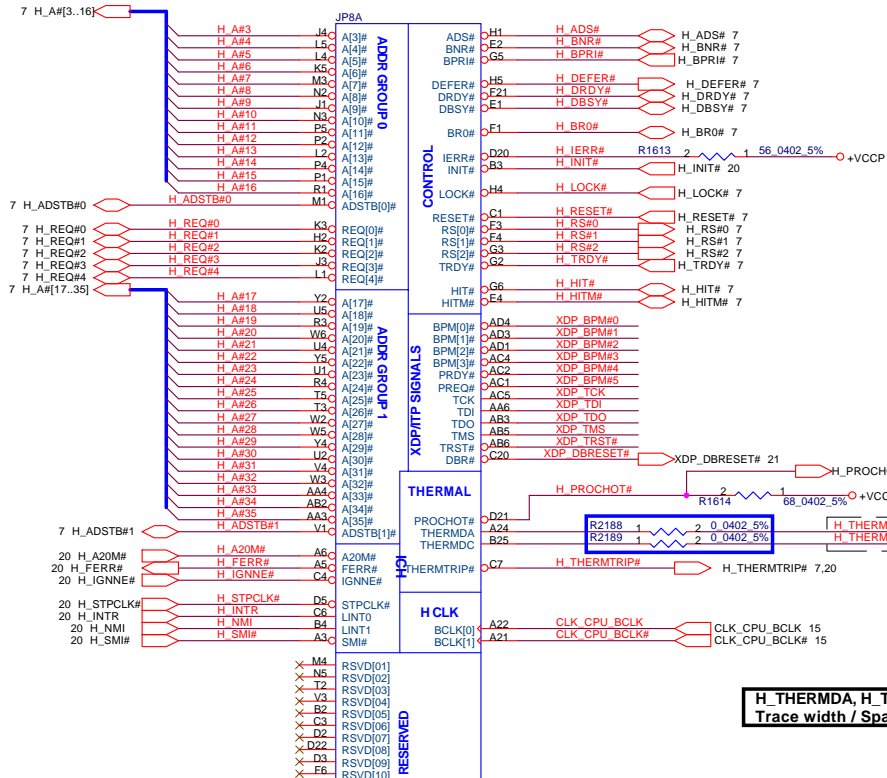
EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

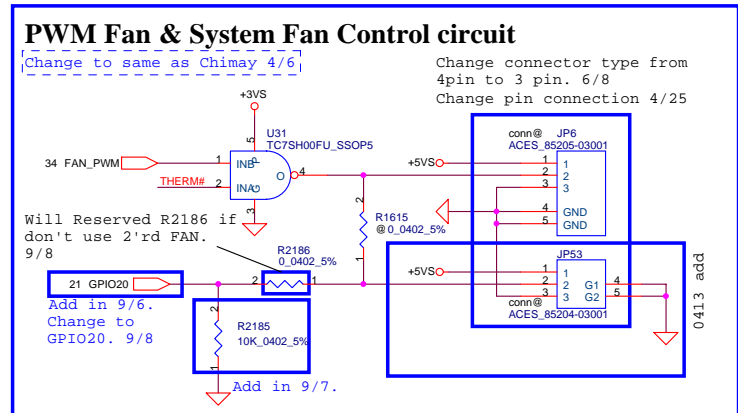
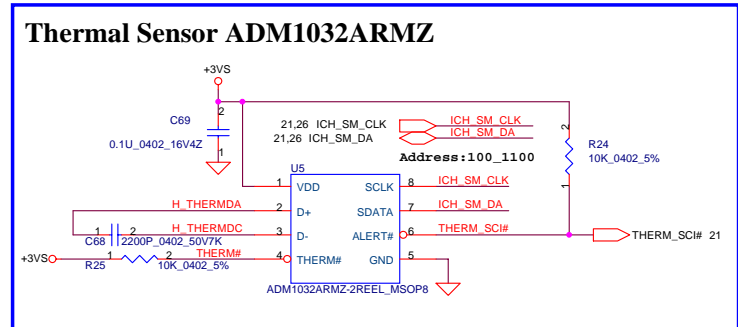
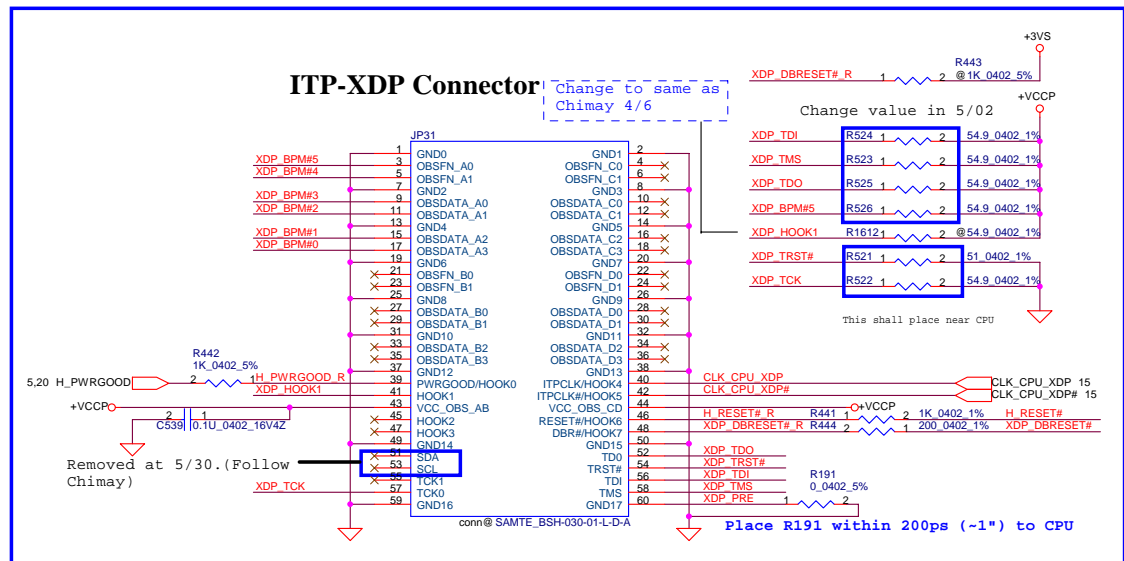
USB PORT#	Destination
0	M/B
1	Finger Printer
2	M/B
3	On Audio Board
4	On Audio Board
5	On Audio Board
6	Blut Tooth
7	Docking
8	On Audio Board
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	<del>Floppy</del>
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass storagage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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				Rev 0.4
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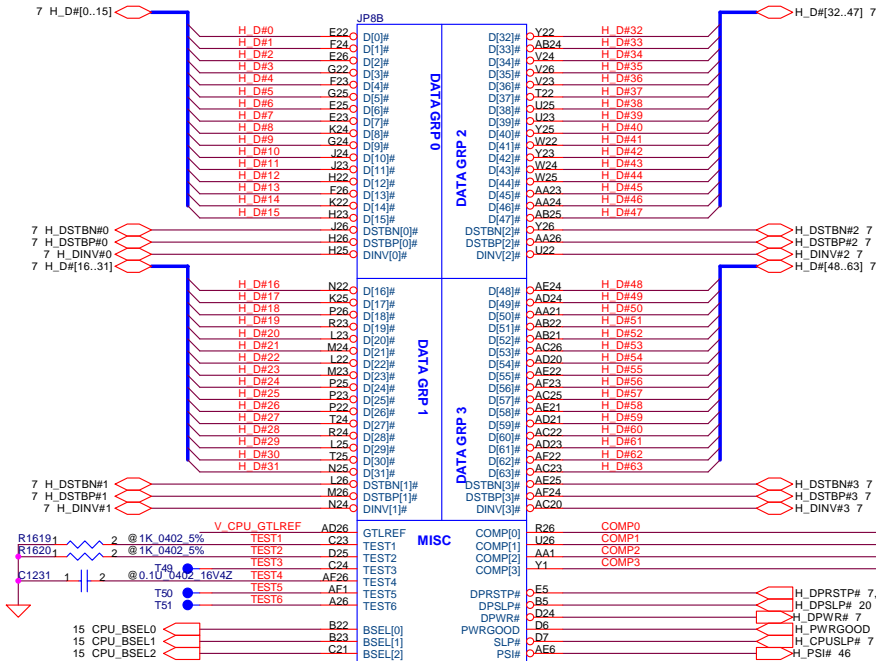


conn@ Merom Ball-out Rev 1a



**H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil**

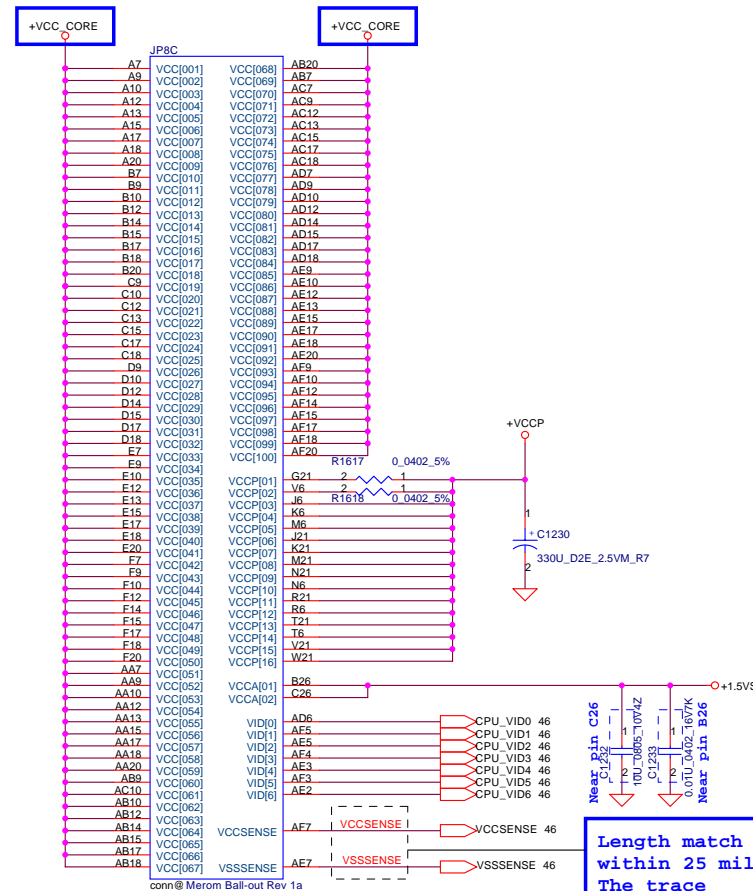
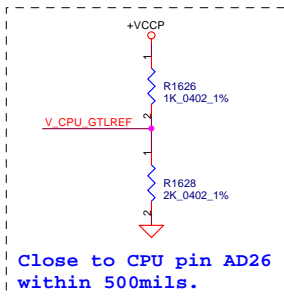
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>Merom(1/3)-AGTL+XDP</b>	
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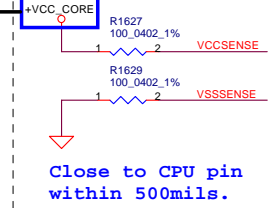
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

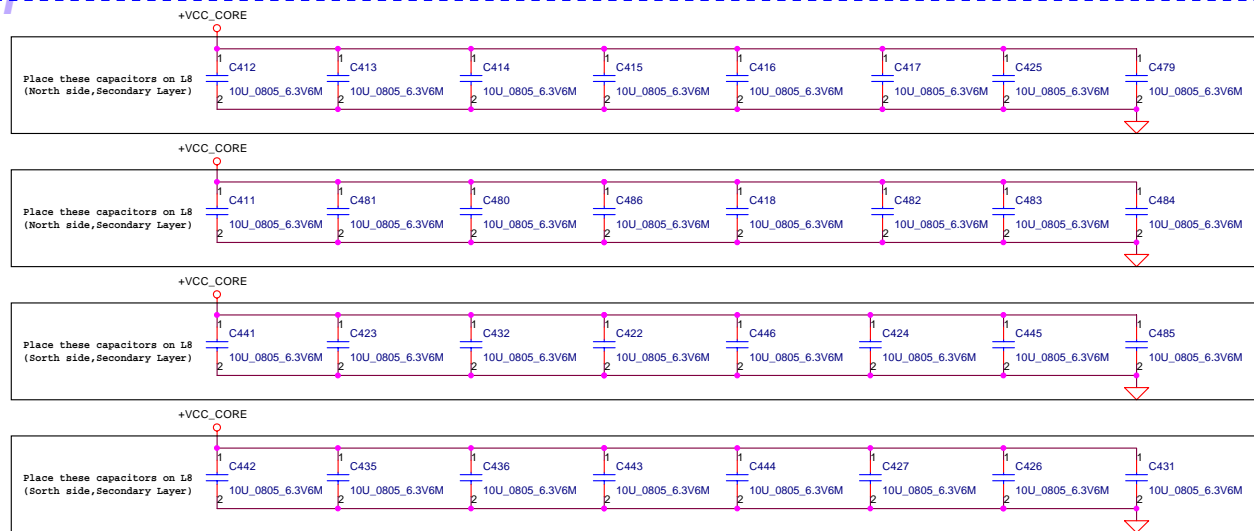
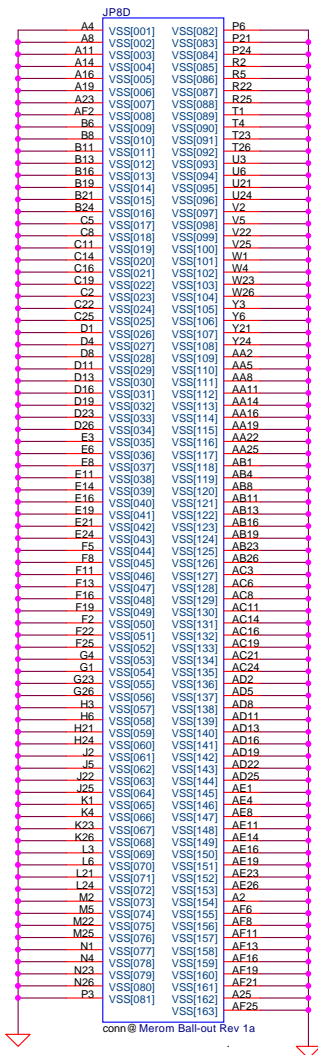
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

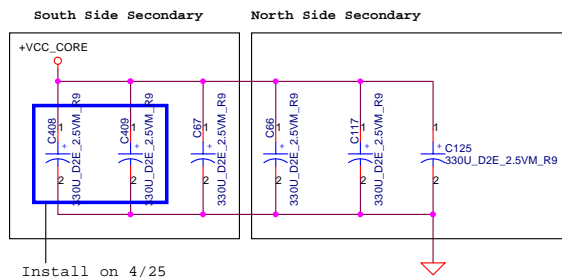


Length match within 25 mils. The trace width/space/other is 20/7/25.

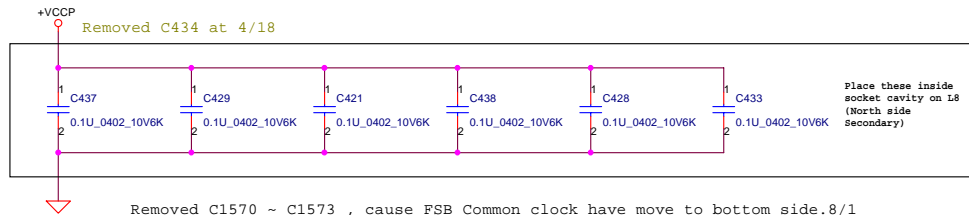




Mid Frequency Decoupling

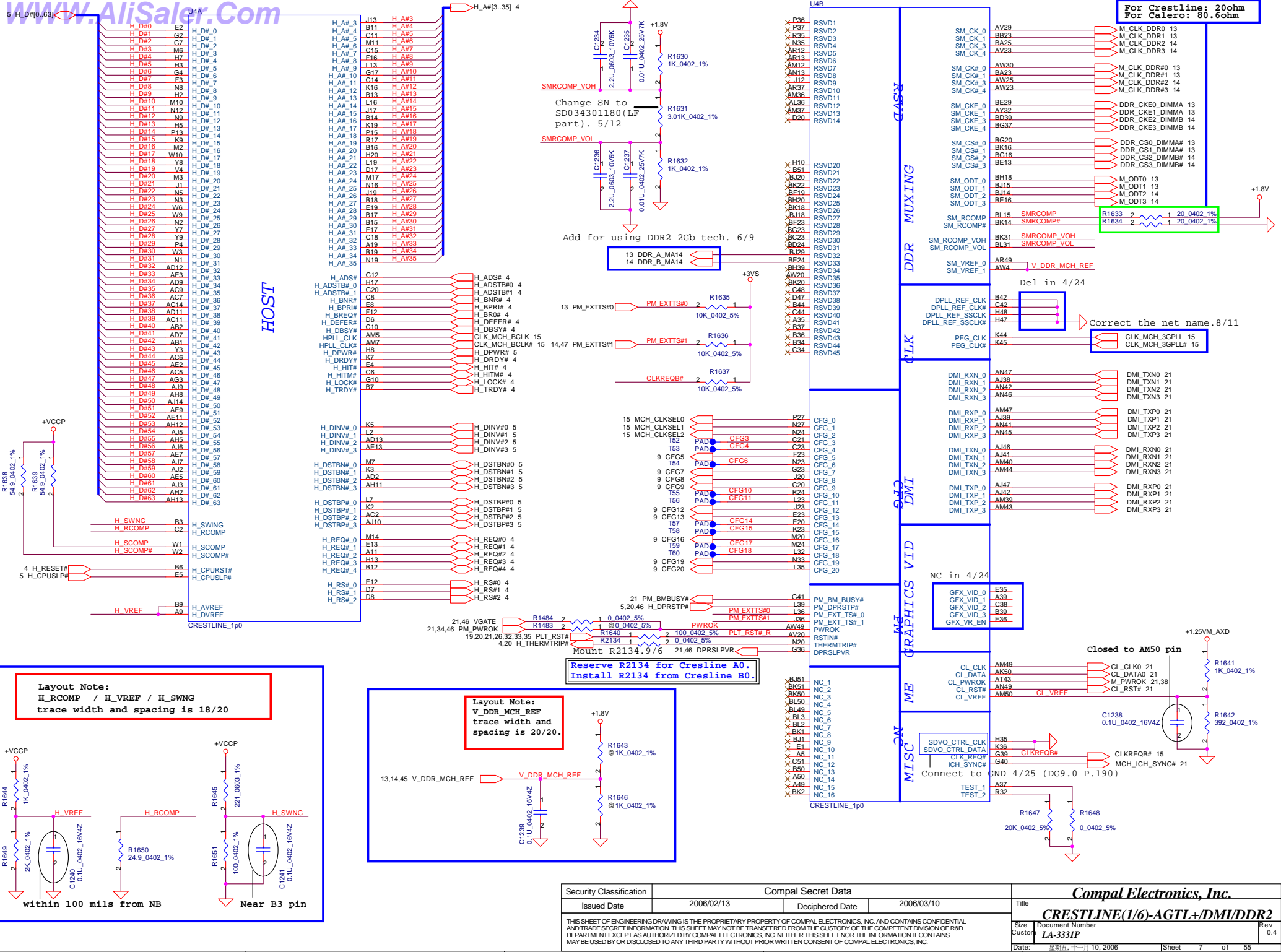


ESR <= 1.5m ohm  
Capacitor > 1980uF

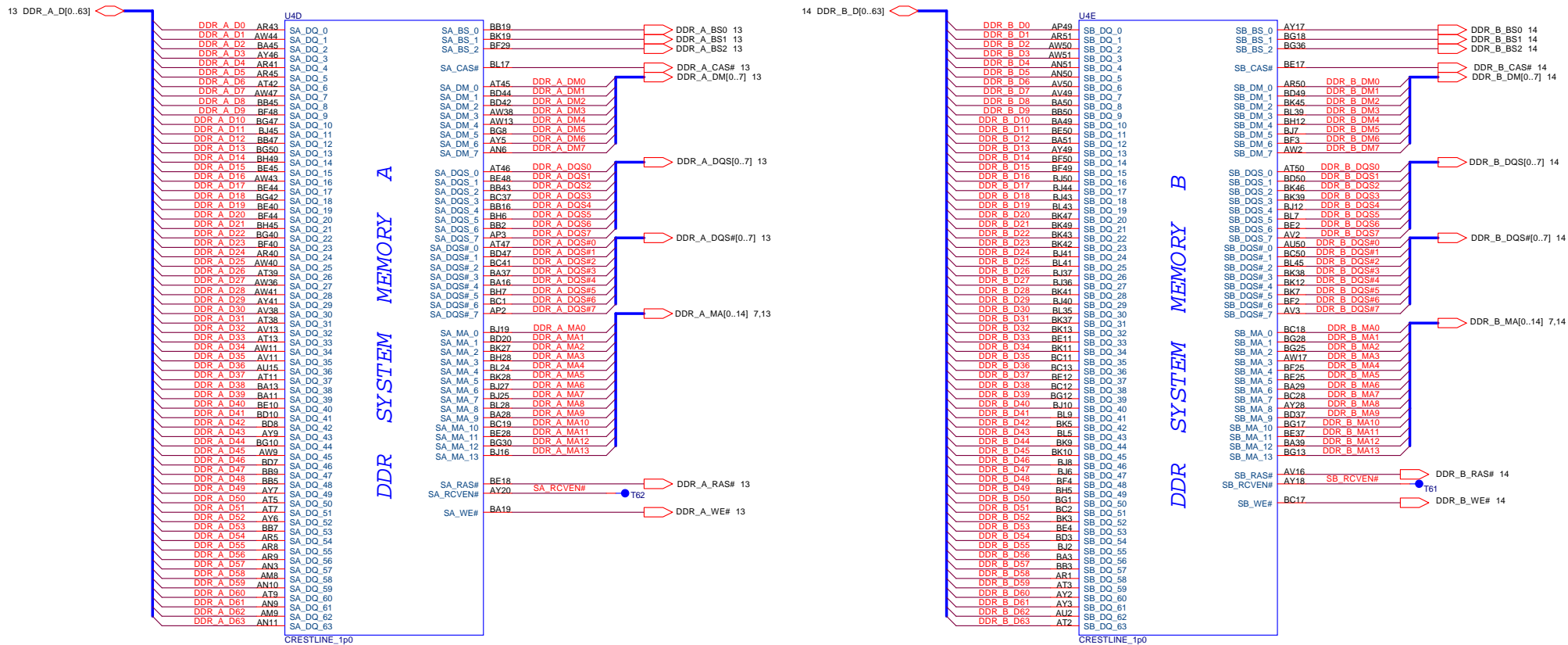


Removed C1570 ~ C1573 , cause FSB Common clock have move to bottom side.8/1

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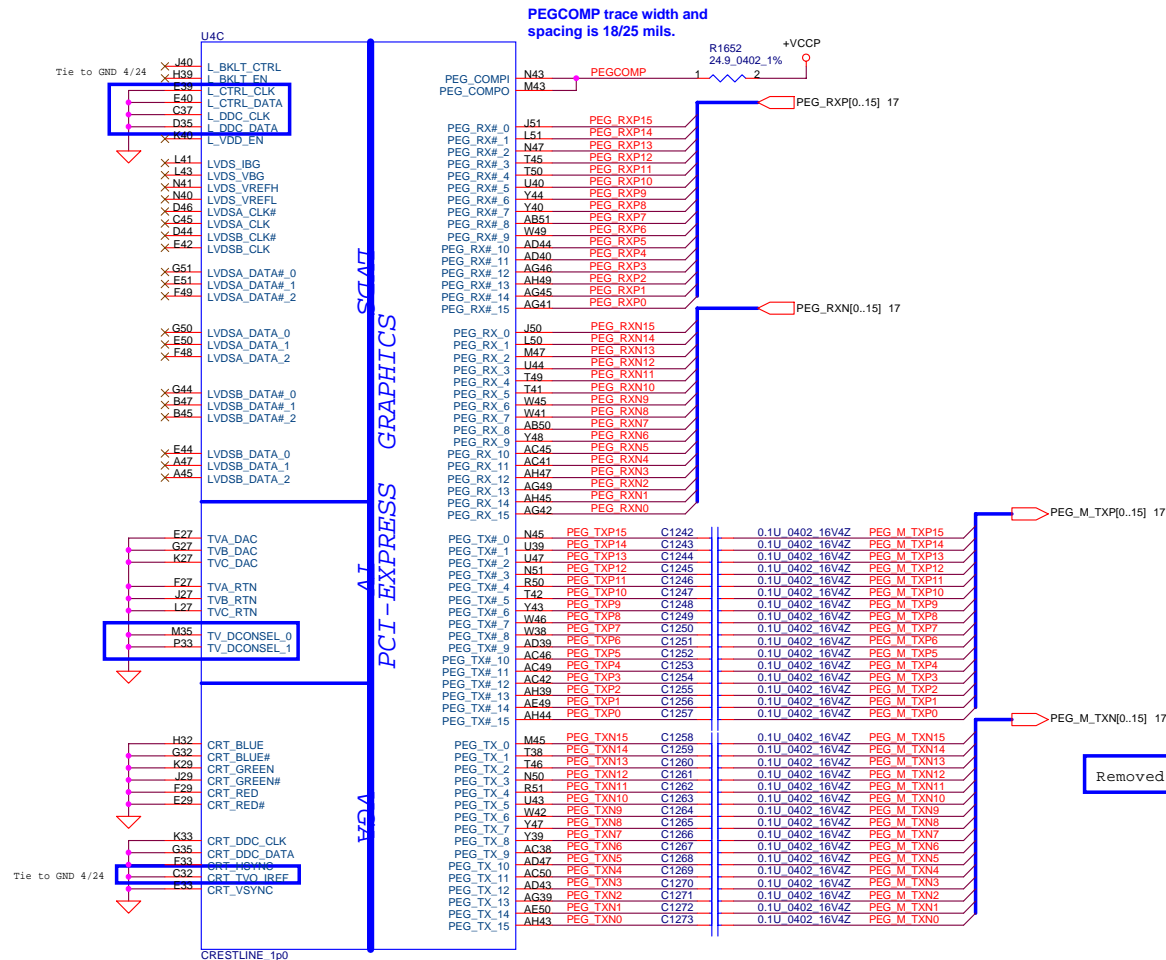
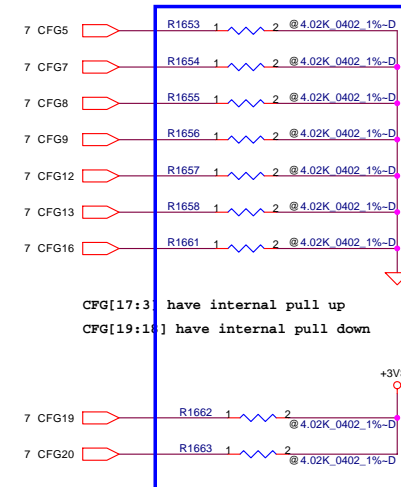
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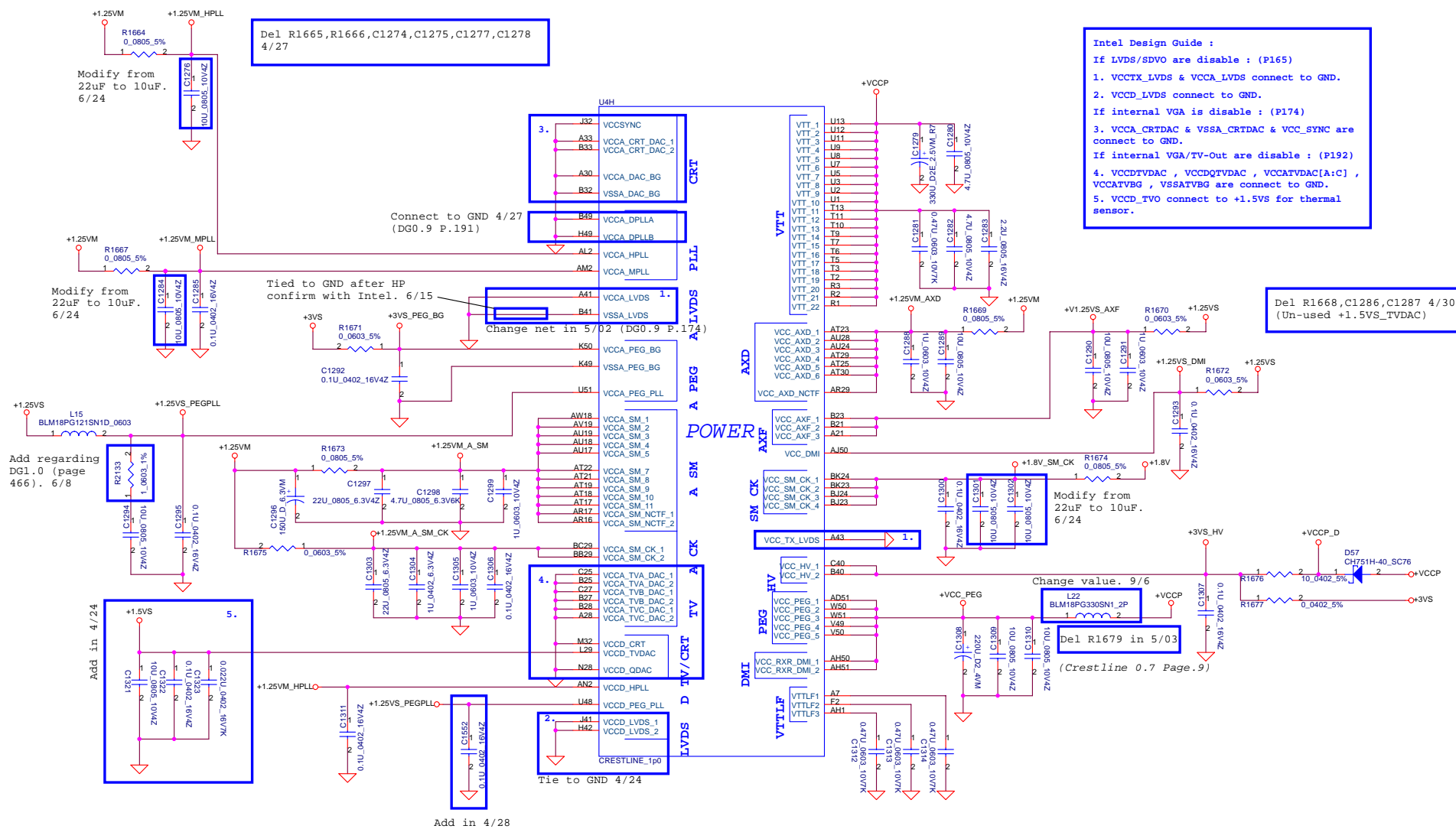


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55		1			

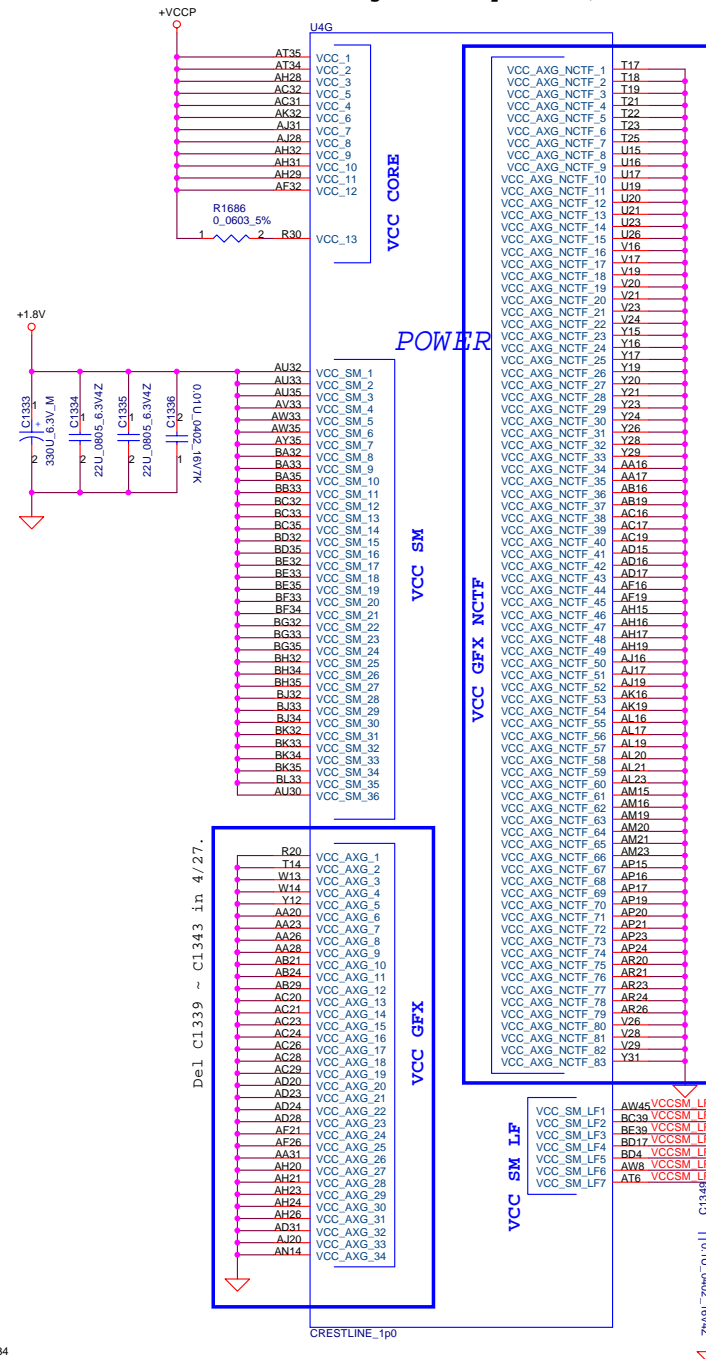
## Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.





Del C1325 ~ C1327 in 4/27.



Del C1339 ~ C1343 in 4/27.

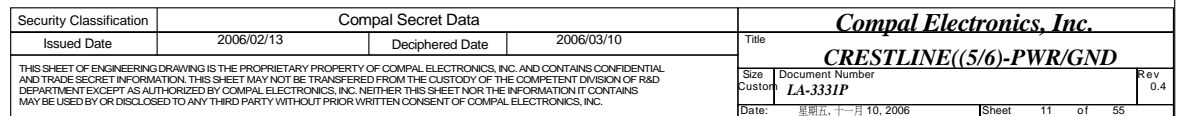
SM

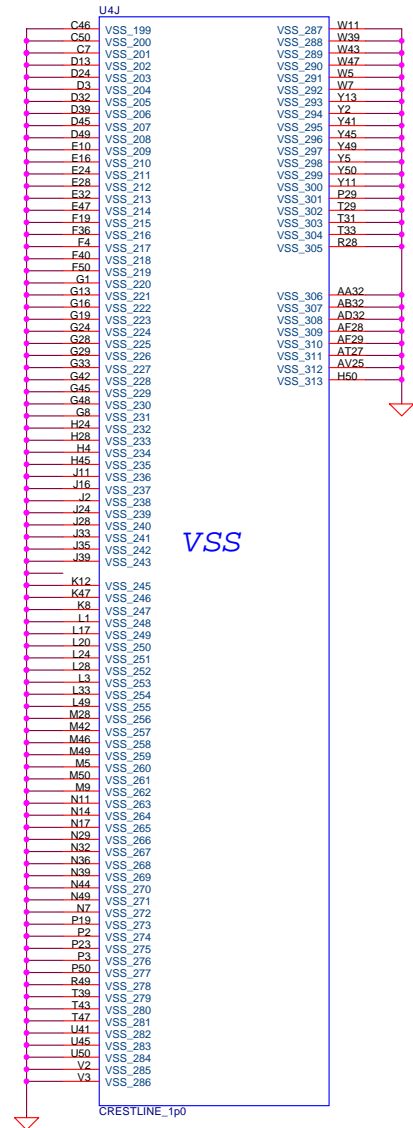
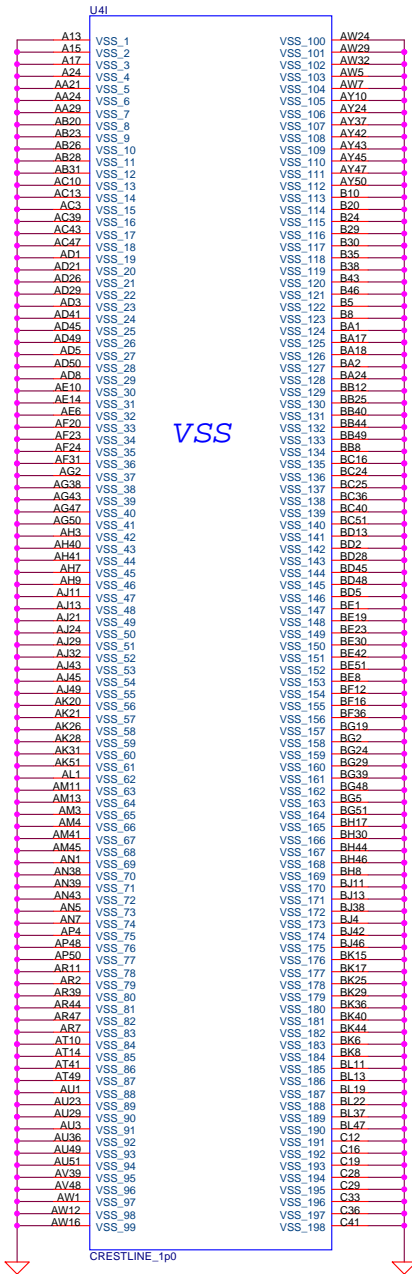
VCC GEX NCTF

VCC GFX

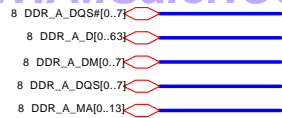
VCC SM LF

CRACK\_BGA 22,34

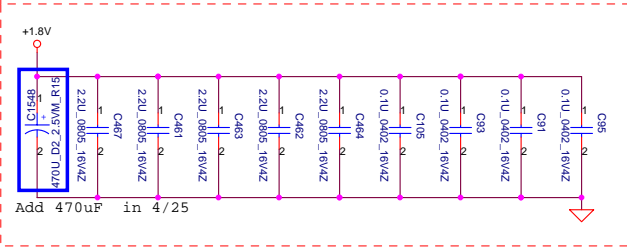




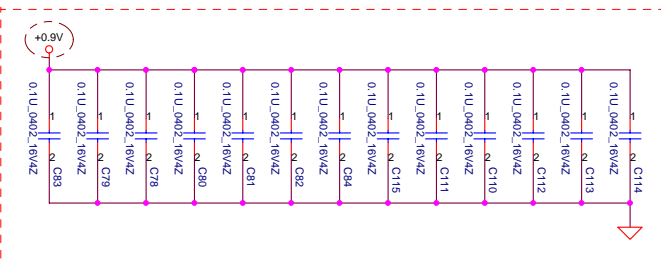
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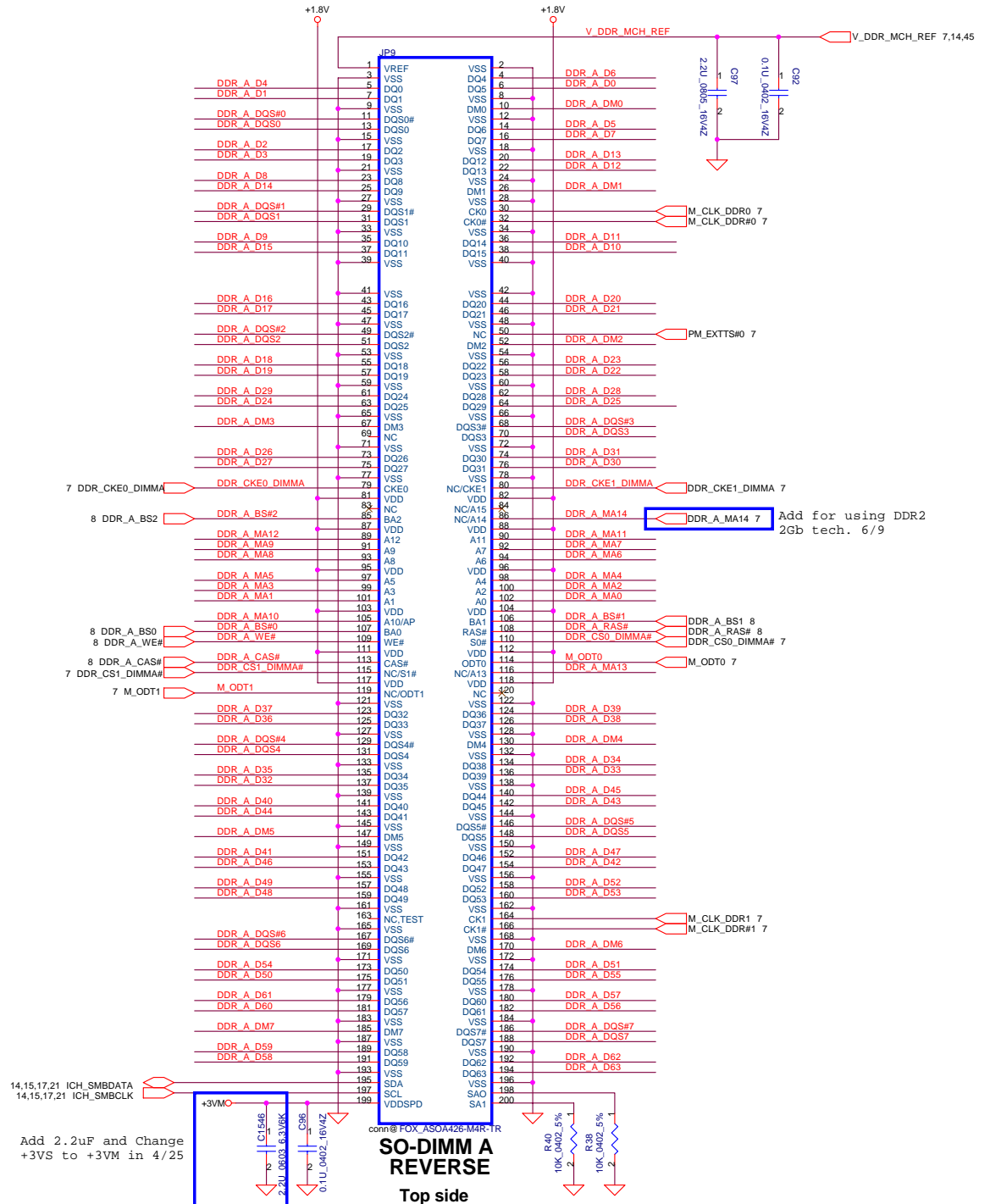
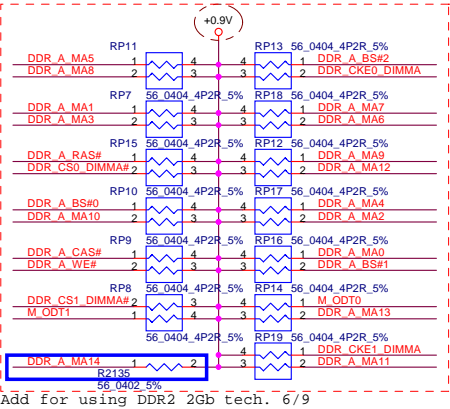
**Layout Note:**  
Place near JP9



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place these resistor closely JP9, all trace length Max=1.5"



14,15,17,21 ICH\_SMBDATA  
14,15,17,21 ICH\_SMBCLK  
Add 2.2uF and Change +3VS to +3VM in 4/25

**SO-DIMM A REVERSE**

Top side

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The diagram shows a 10-bit DAC implemented with a resistor ladder network. A +0.9V input is connected to a series of resistors labeled C471 through C479. The output of the ladder is connected to a common ground, indicated by a red arrow.

Diagram illustrating the memory layout and access patterns for DDR B MA1 and DDR B MA2, showing the mapping of memory banks (RP34, RP35, RP6, RP3, RP2, RP36, RP37) and the resulting data flow (DDR B MA9, DDR B MA12, DDR B BS#0, DDR B MA10, DDR B MA0, DDR B BS#1, DDR B CAS#, DDR B WE#, DDR CS3 DIMMB#2, M\_ODT3, DDR B MA14, DDR B BS#2, DDR CKE2 DIMMB).

The diagram shows the mapping of memory banks (RP34, RP35, RP6, RP3, RP2, RP36, RP37) and the resulting data flow (DDR B MA9, DDR B MA12, DDR B BS#0, DDR B MA10, DDR B MA0, DDR B BS#1, DDR B CAS#, DDR B WE#, DDR CS3 DIMMB#2, M\_ODT3, DDR B MA14, DDR B BS#2, DDR CKE2 DIMMB). The diagram is divided into two main sections, each with a 5/16 ratio. The left section shows the mapping of DDR B MA1 and DDR B MA2 to DDR B BS#0 and DDR B MA10, and the right section shows the mapping of DDR B MA0 and DDR B BS#1 to DDR B CAS# and DDR B WE#.

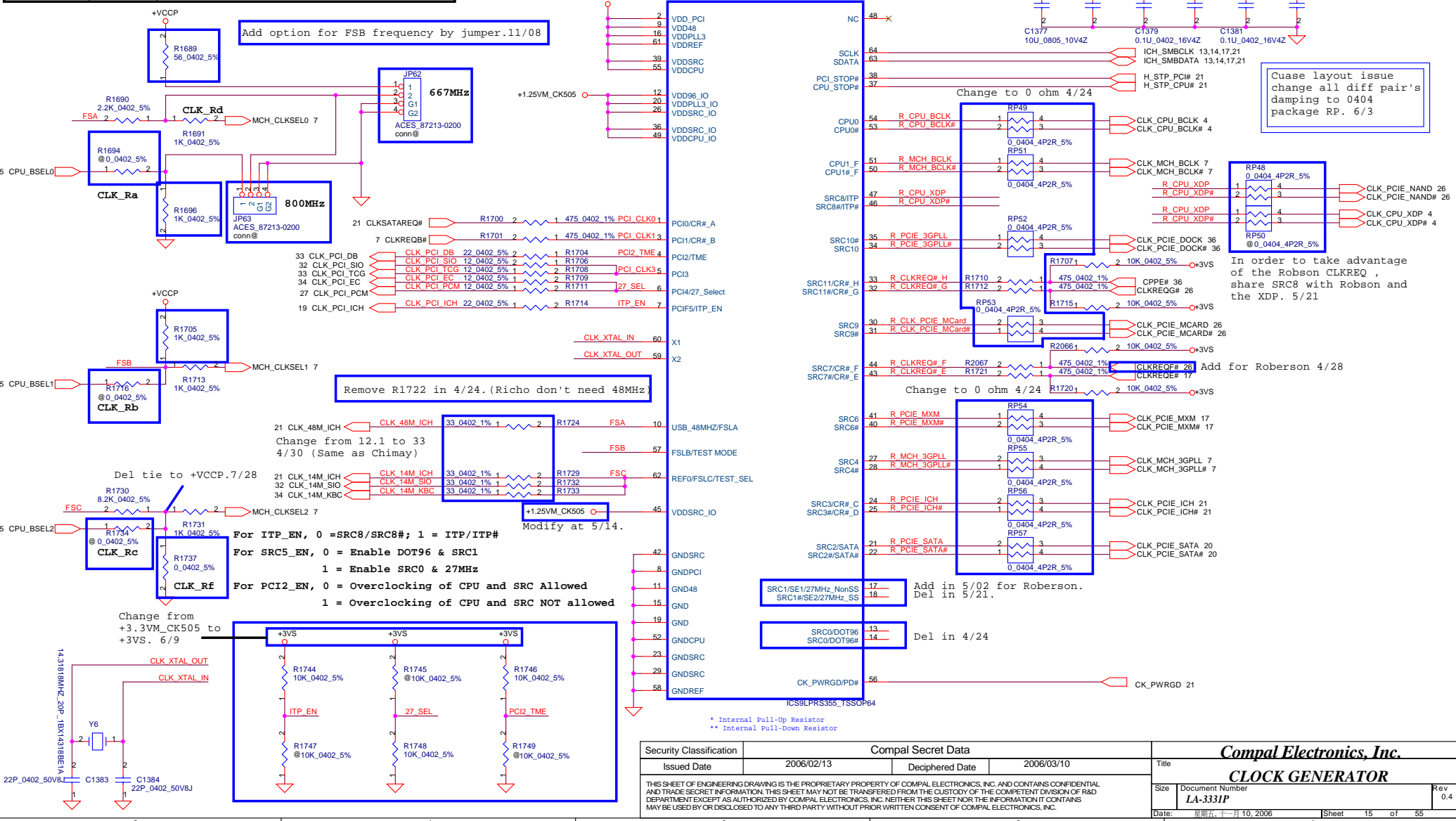
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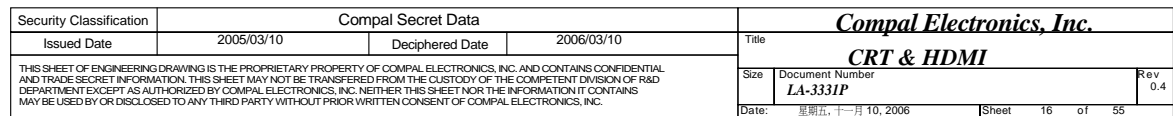
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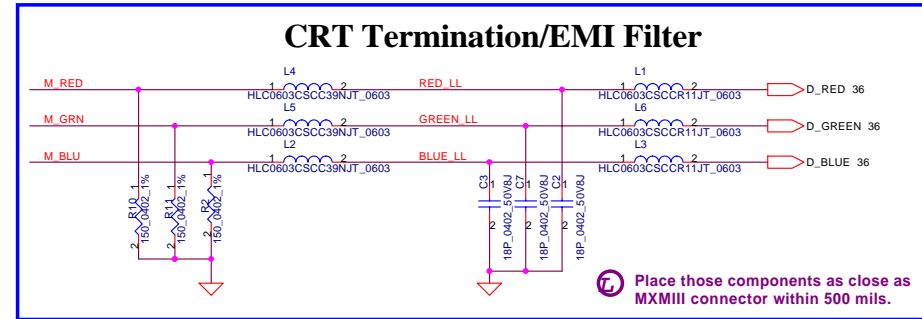
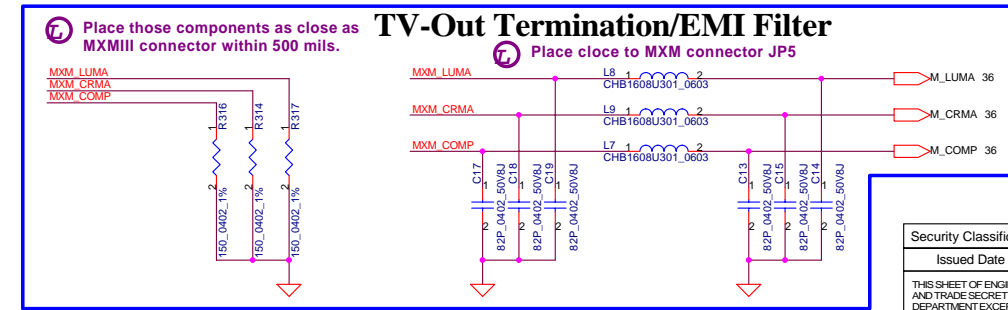
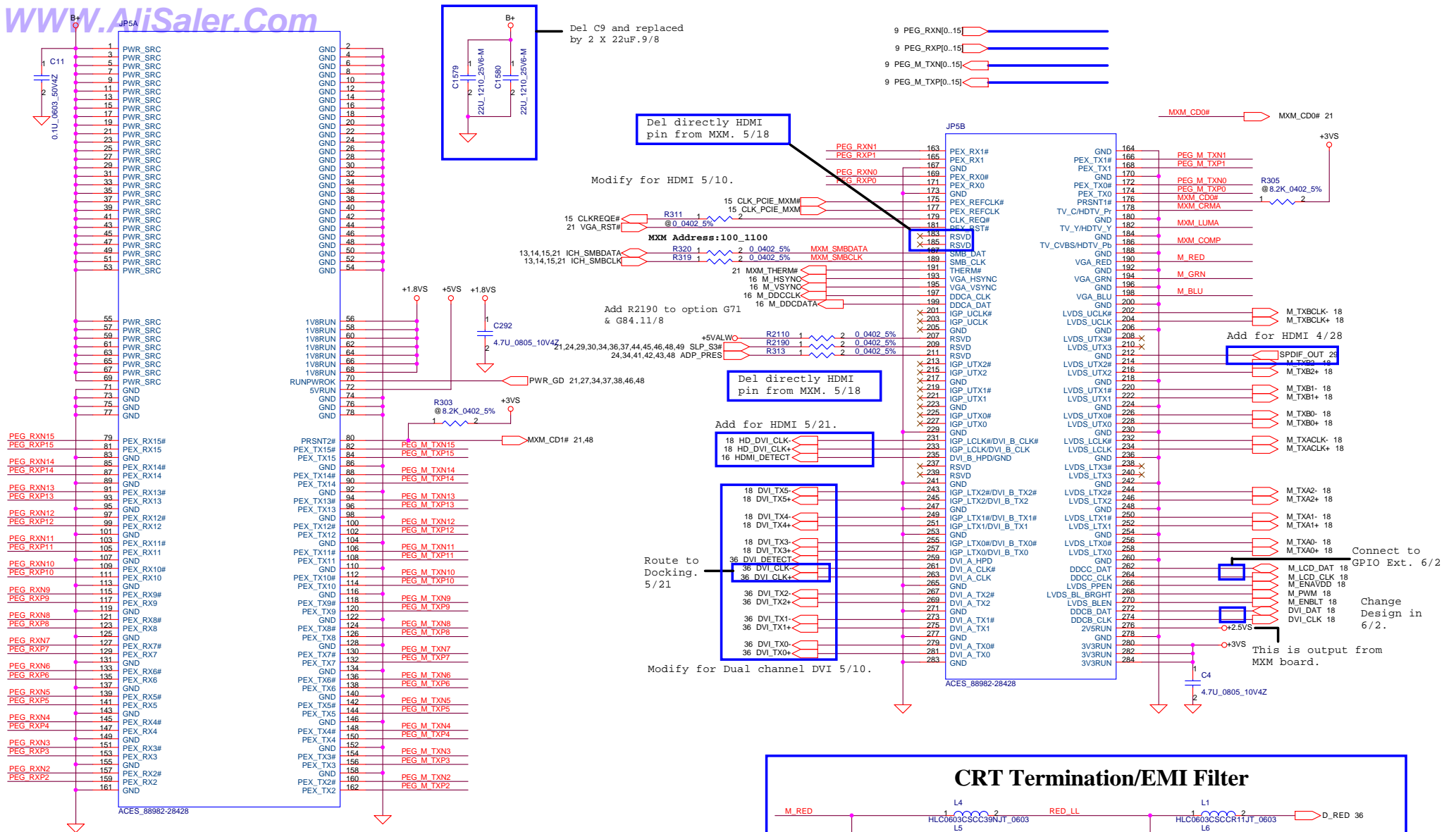
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1694	R1716	R1734
* (Default)	No Stuff	R1689	R1696	R1705 R1719 R1726 R1737
667MHz	Stuff	R1689	R1696	R1734 R1737
	No Stuff	R1694	R1705 R1716 R1719	R1726
800MHz	Stuff		R1734 R1737	
	No Stuff	R1689 R1694 R1696	R1705 R1716 R1726	R1719

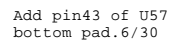
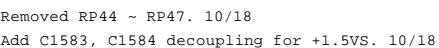
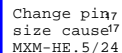






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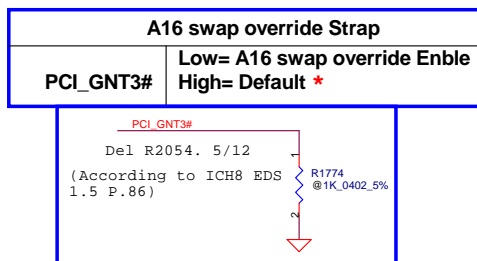
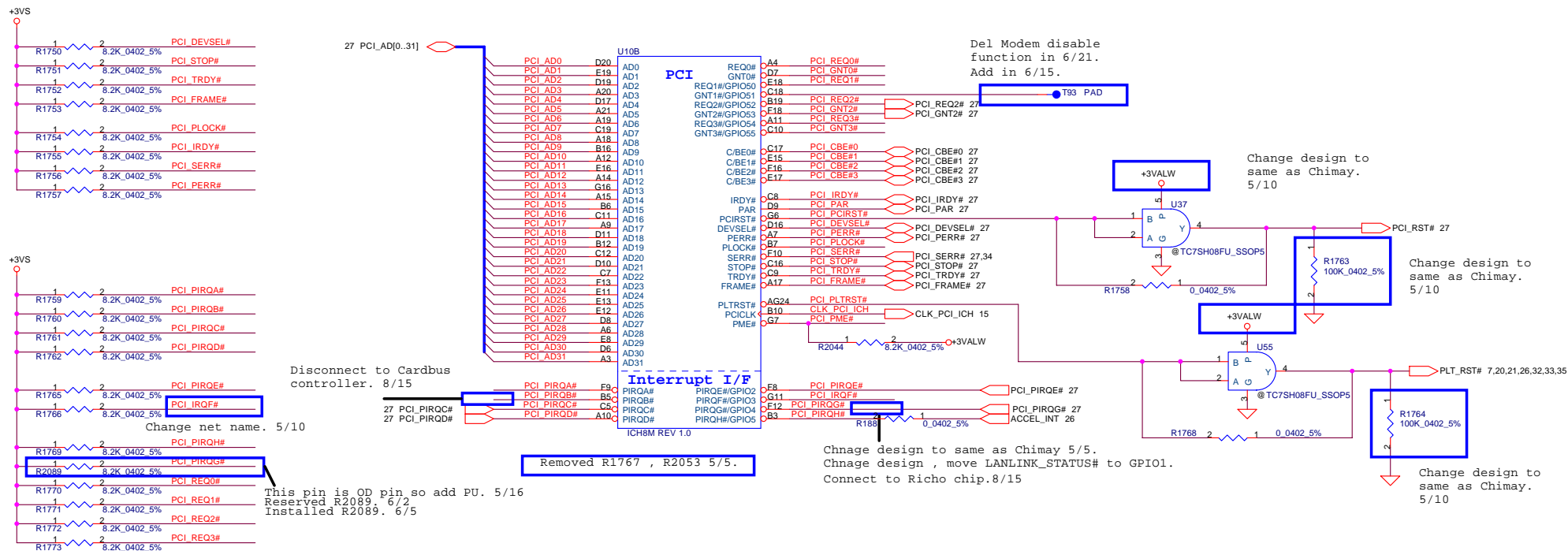
## MXM LVDS CONN



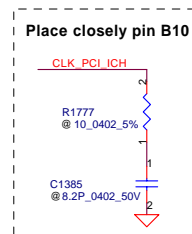
## LCD POWER CIRCUIT

[illegible]

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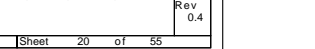
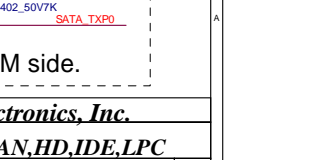
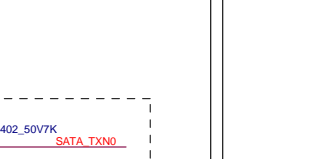
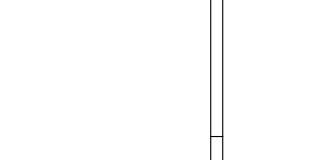
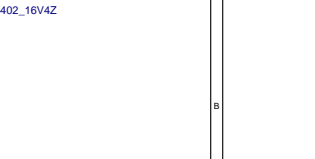
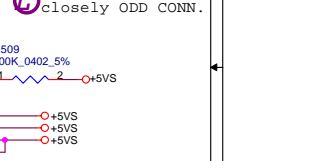
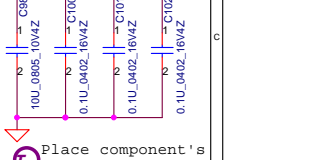
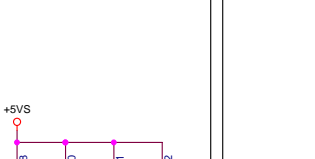
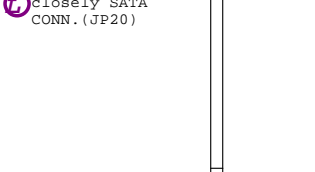
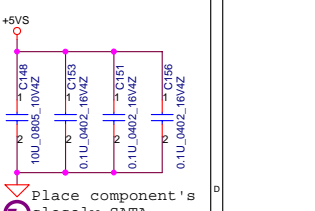
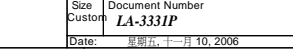
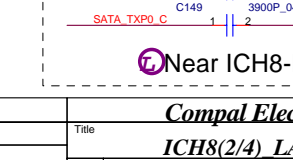
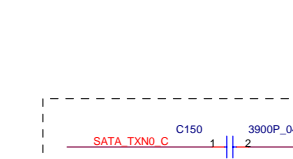
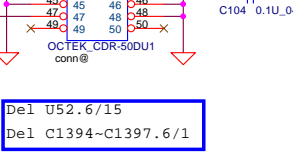
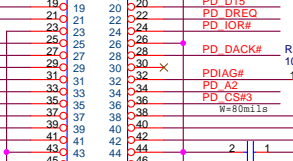
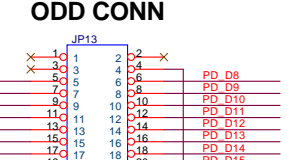
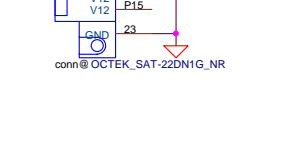
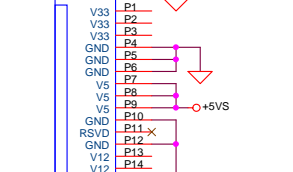
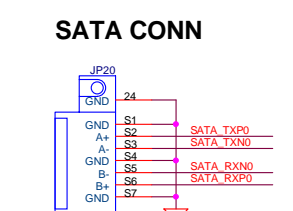
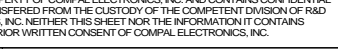
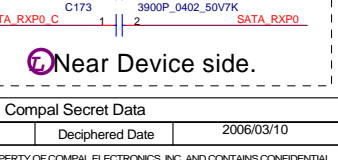
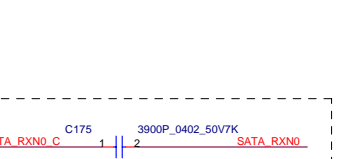
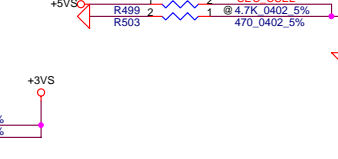
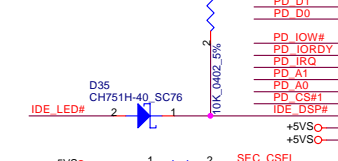
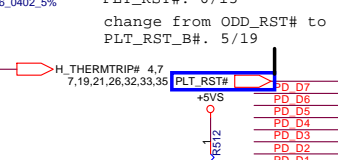
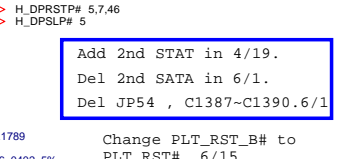
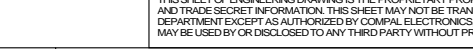
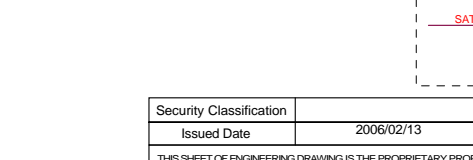
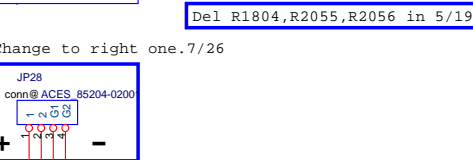
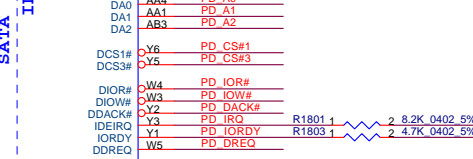
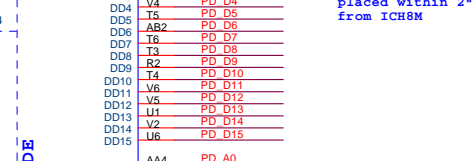
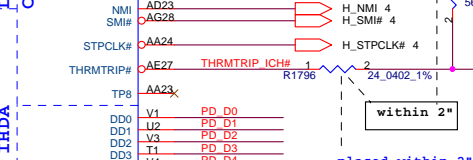
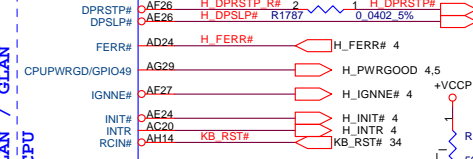
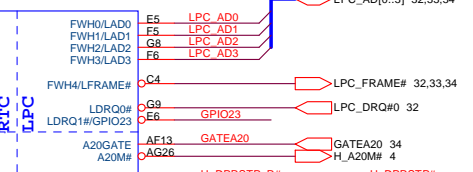
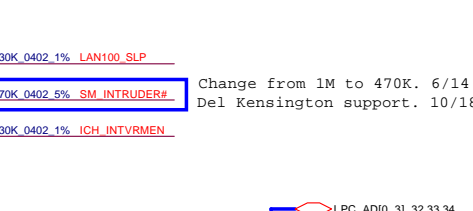
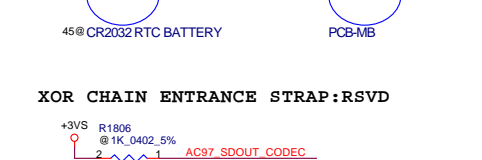
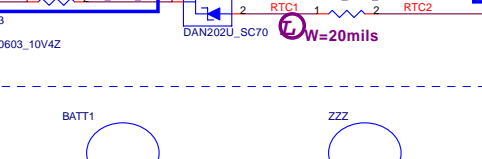
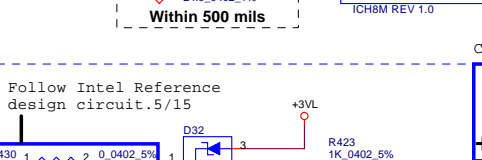
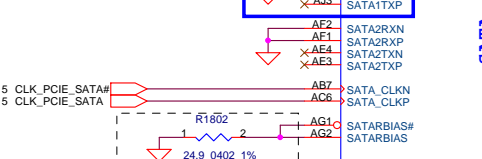
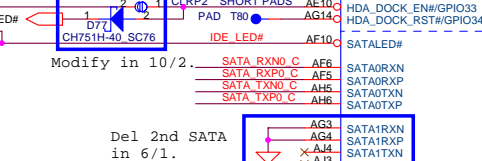
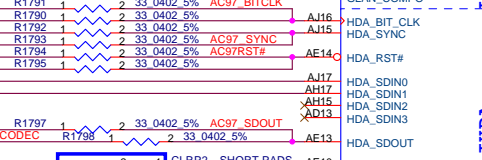
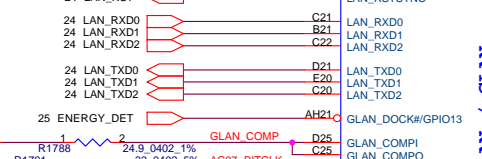
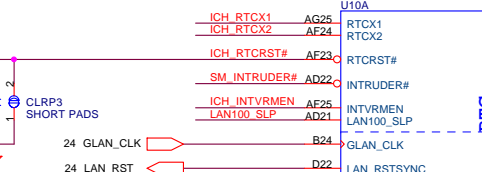
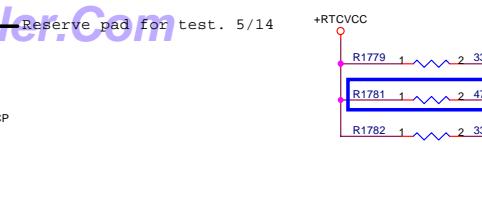
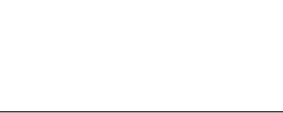
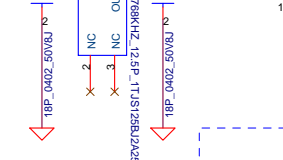
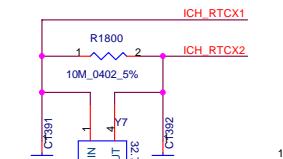
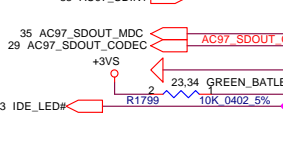
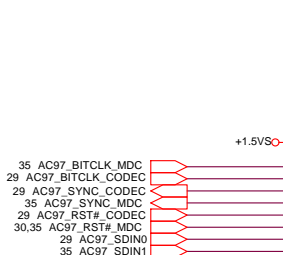
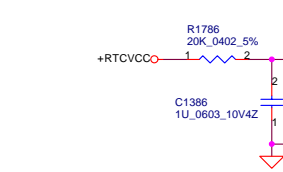
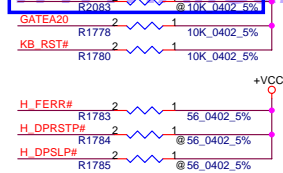


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



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				Size	Document Number	Rev
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Date:				星期日, 十一月 10, 2006	Sheet 19 of 55	

WWW.AJSHI.COM Reserve pad for test. 5/14



Change from 1M to 470K. 6/14  
Del Kensington support. 10/18

Add 2nd STAT in 4/19.  
Del 2nd SATA in 6/1.  
Del JP54 , C1387-C1390.6/1

Change PLT\_RST\_B# to  
PLT\_RST#. 6/15  
change from ODD\_RST# to  
PLT\_RST\_B#. 5/19

within 2"

placed within 2"  
from ICH8M

Del R1804,R2055,R2056 in 5/19.

Change to right one.7/26

Follow Intel Reference  
design circuit.5/15

W=20mils

W=80mils

W=20mils

W=20mils

Place component's  
closely SATA  
CONN. (JP20)

Place component's  
closely ODD CONN.

Place component's  
closely ODD CONN.

Place component's  
closely ODD CONN.

Place component's  
closely ODD CONN.

Place component's  
closely ODD CONN.

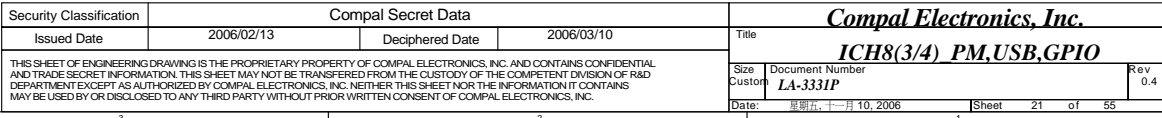
Place component's  
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Place component's  
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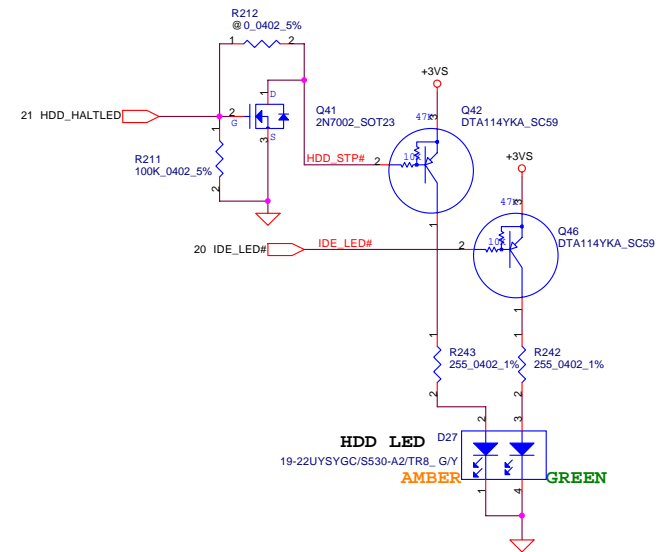
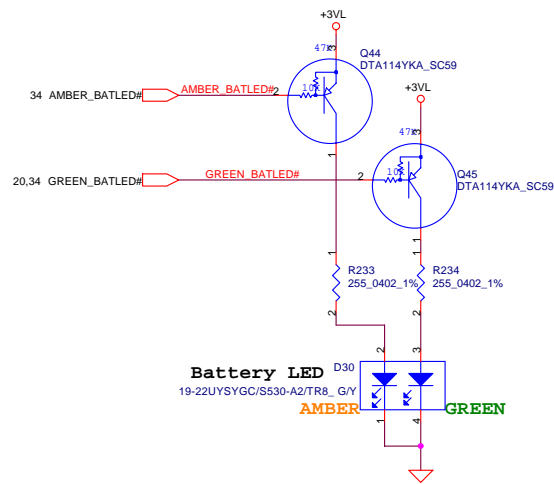
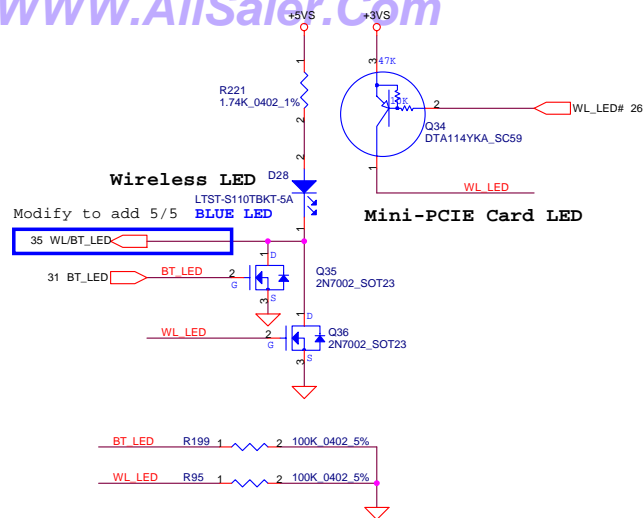
Place component's  
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Place component's  
closely ODD CONN.

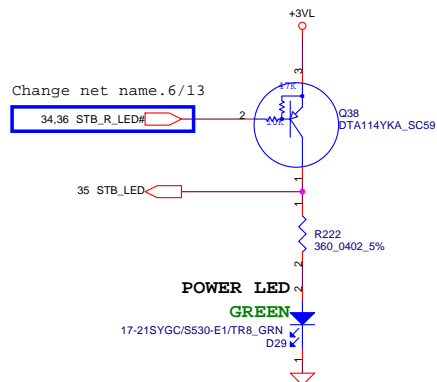
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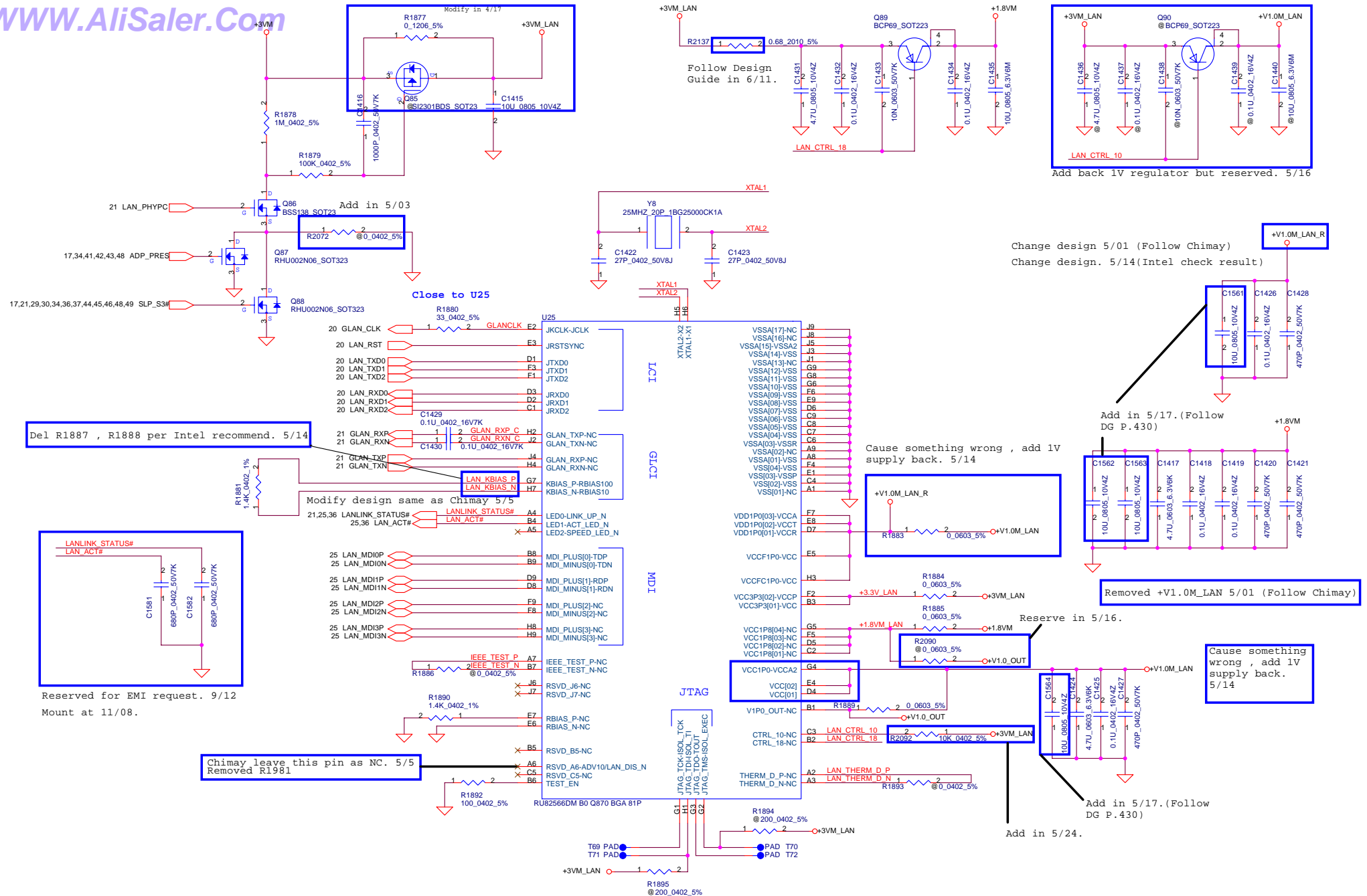
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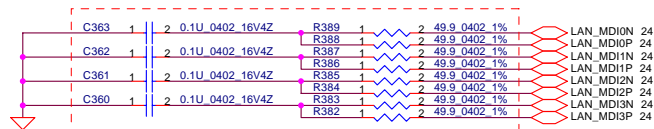
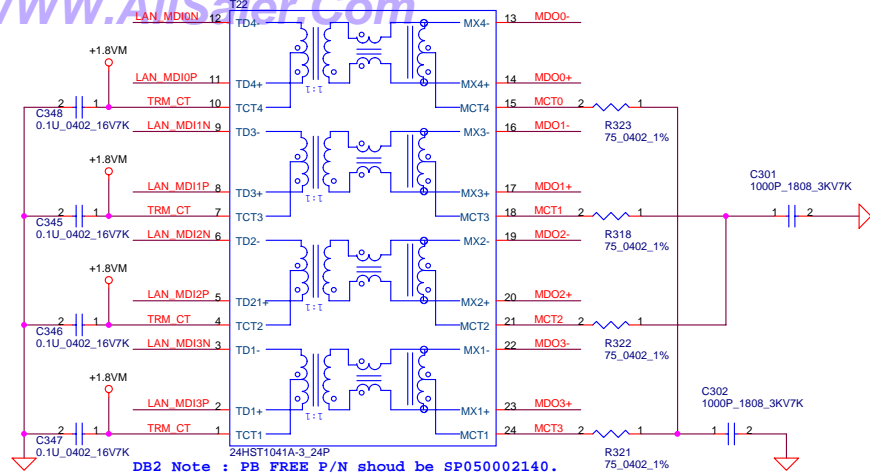
Del R2109. 6/14  
Add the kill circuit.5/25  
Update design. 5/14  
Reserved Space for Kensington 4/27  
Removed Kensington 10/18.



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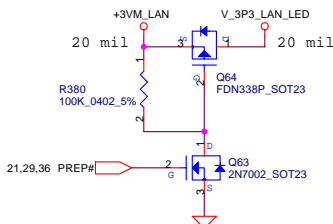
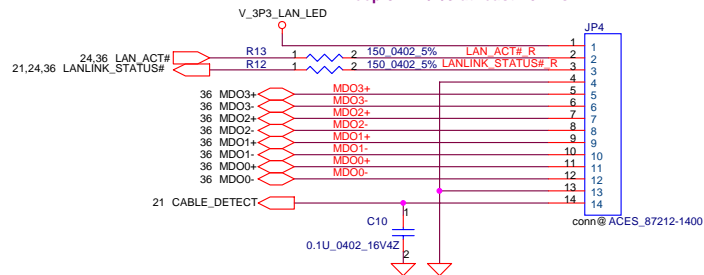
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
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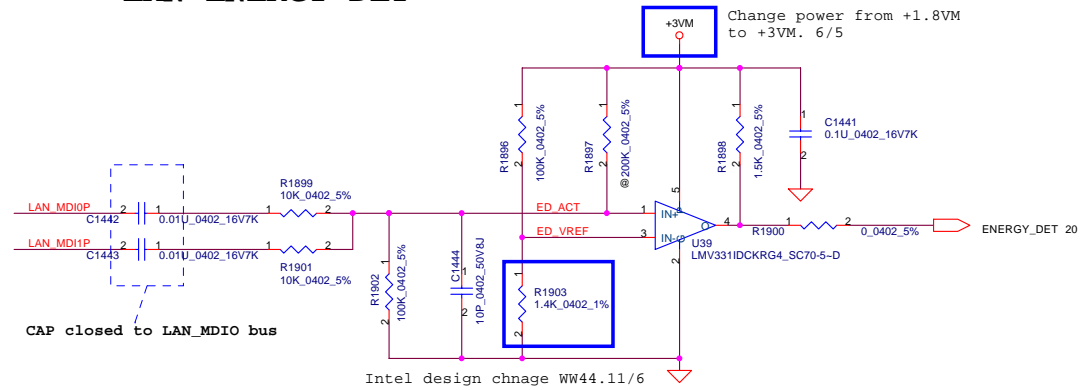
Layout Notice : Place termination as close as Intel 82566 as possible

## To RJ-45 CONN.

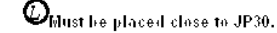
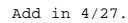
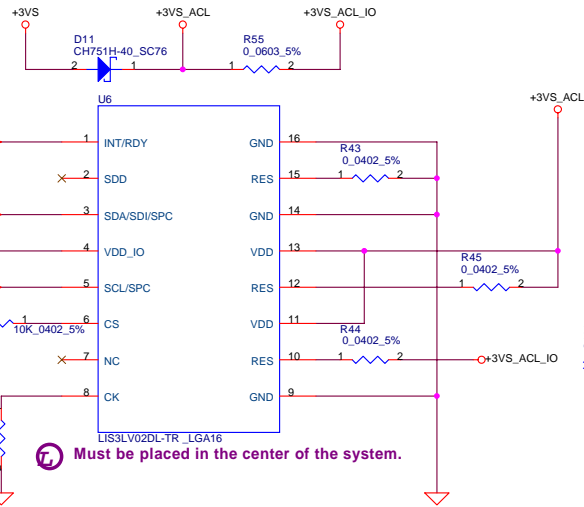
Keep JP4.1/2/3 at least 10mils



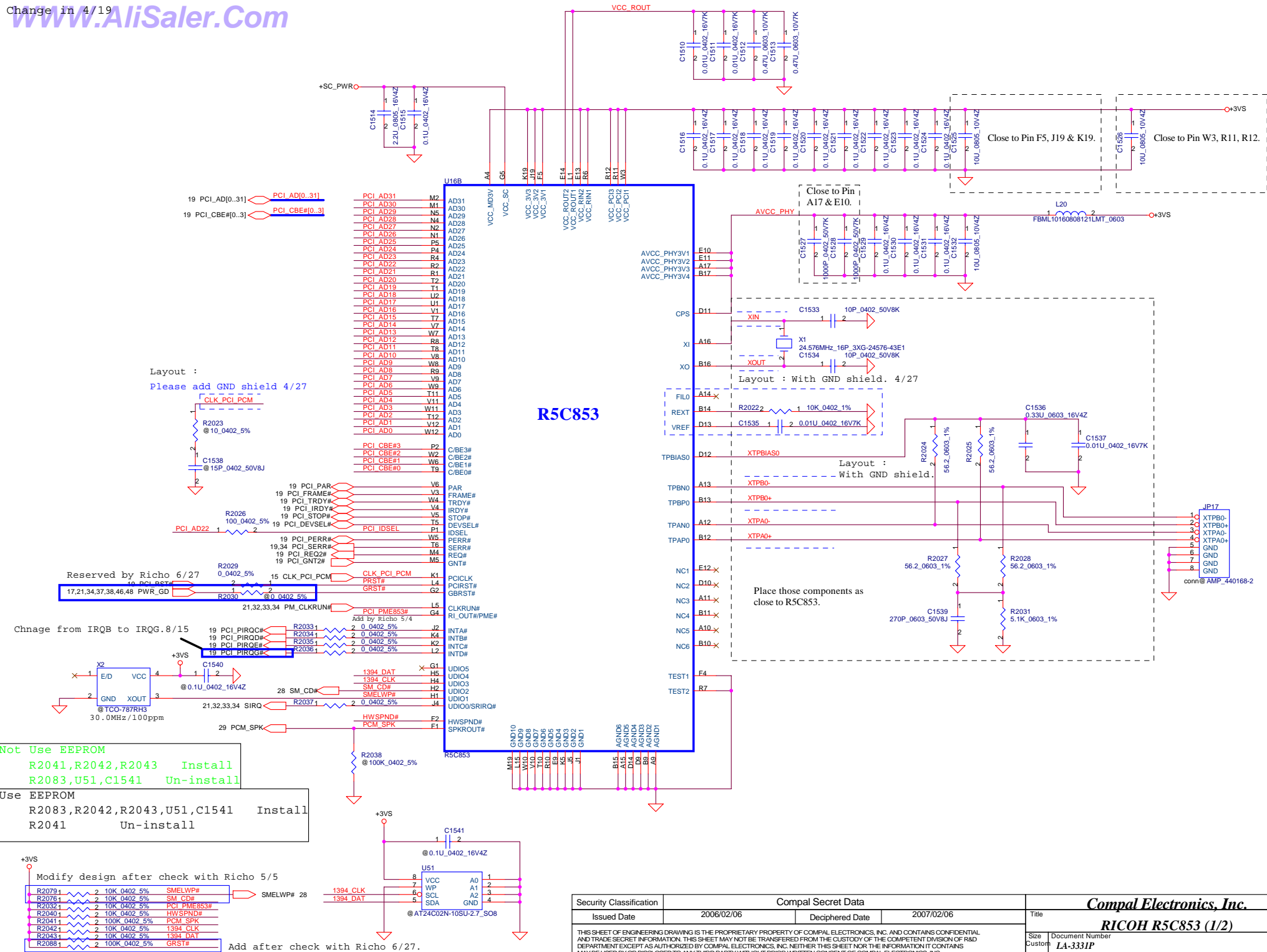
## LAN ENERGY DET



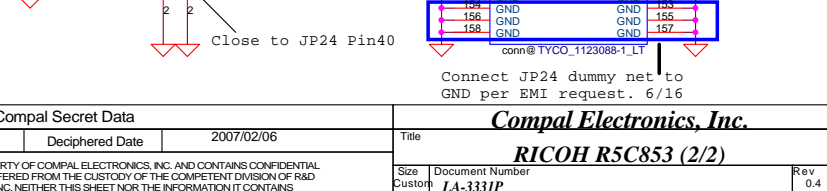
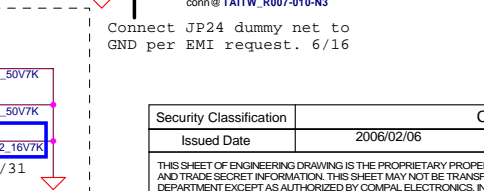
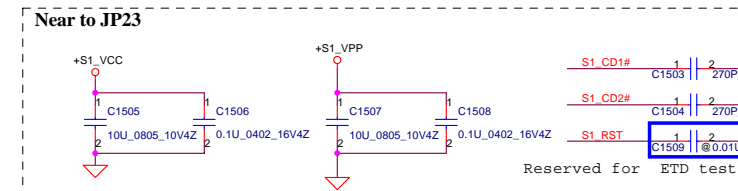
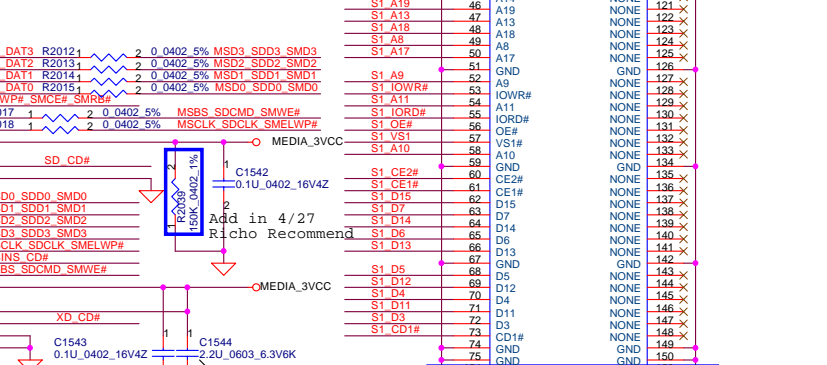
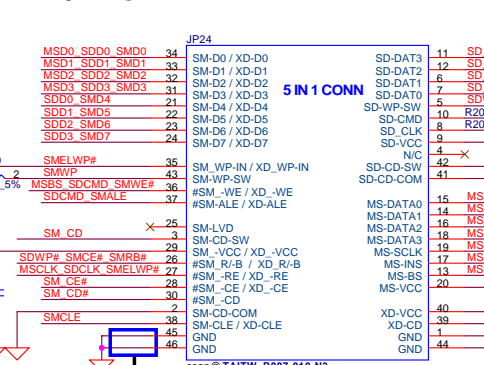
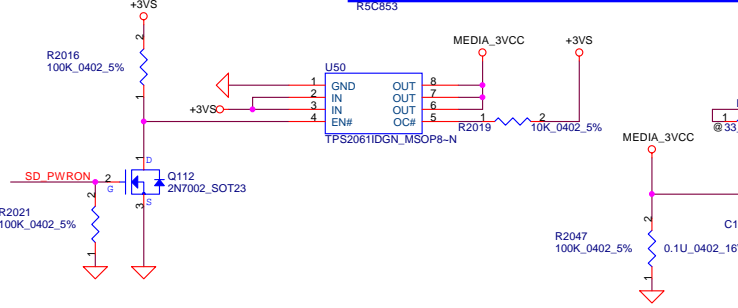
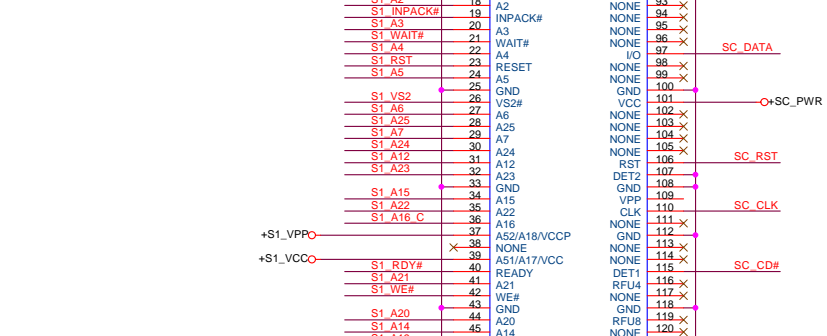
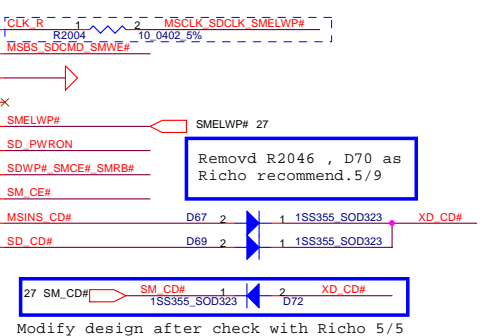
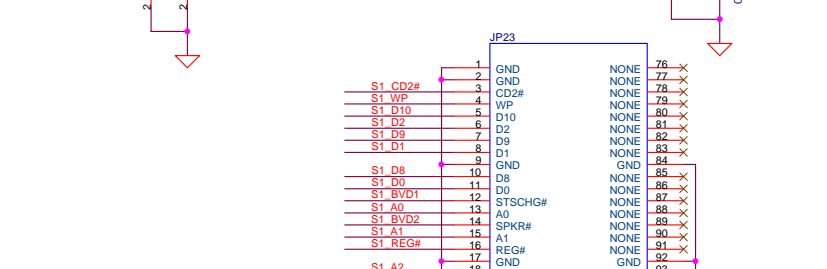
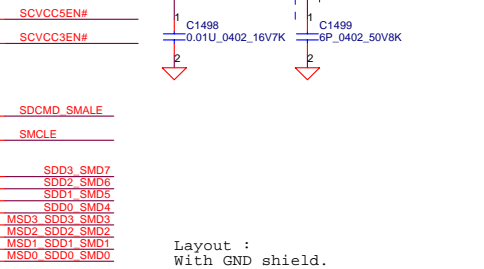
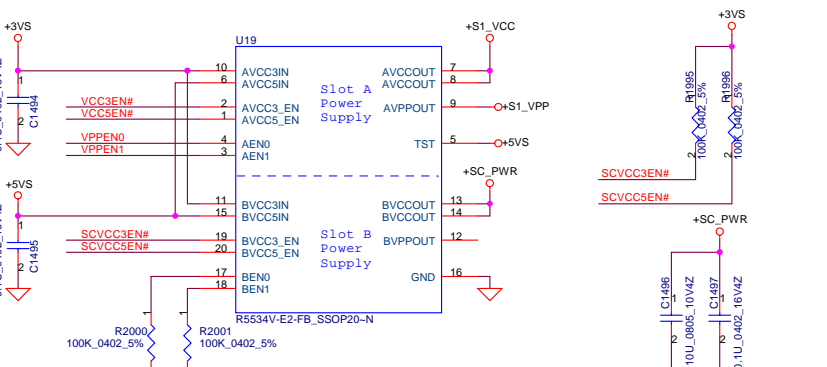
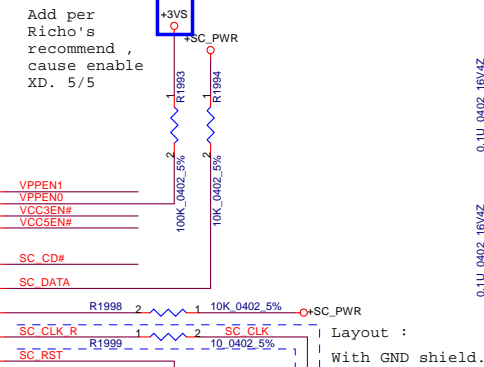
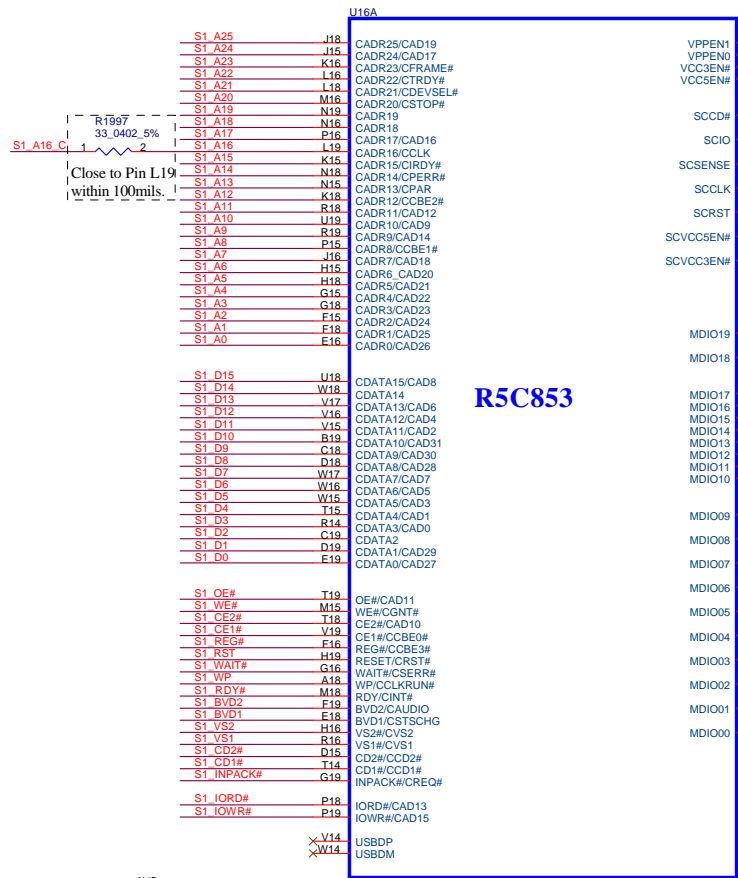
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				星期二, 十一月 10, 2006	0.4
				Sheet	25 of 55



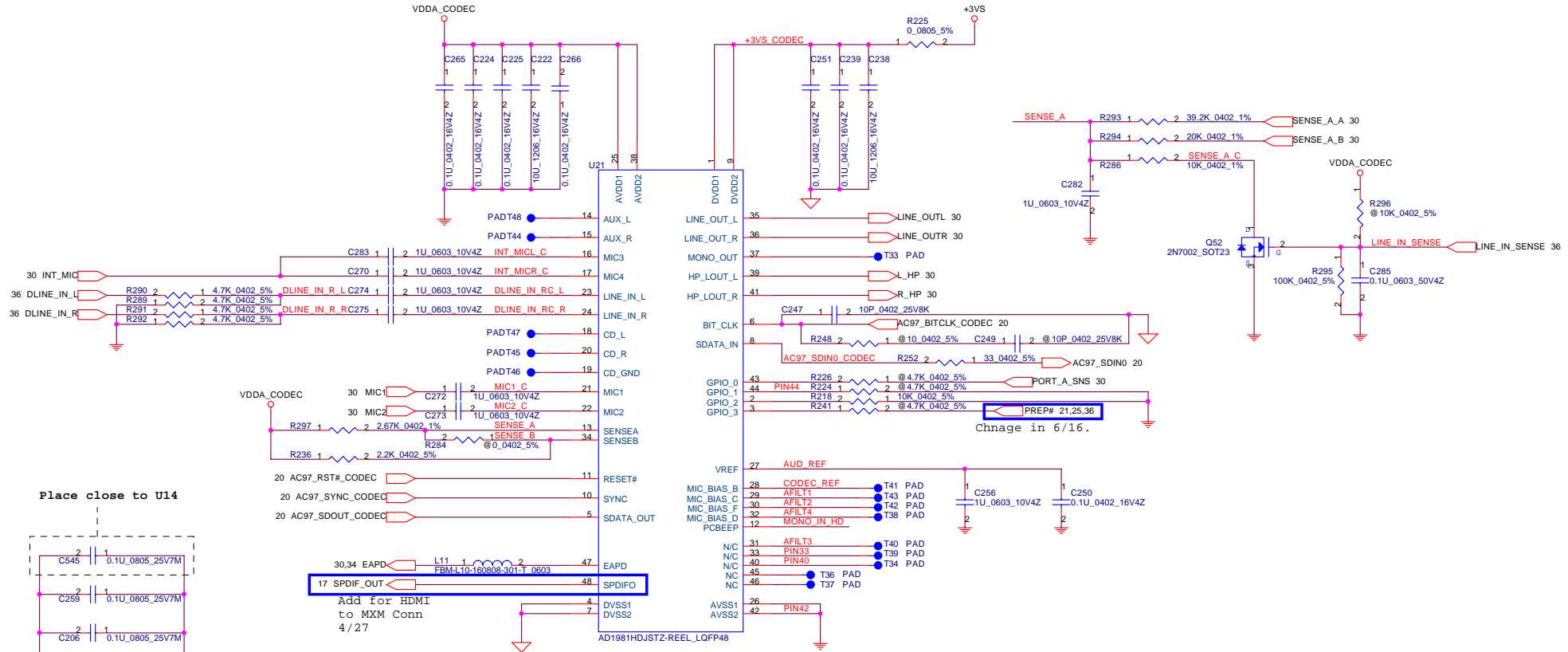
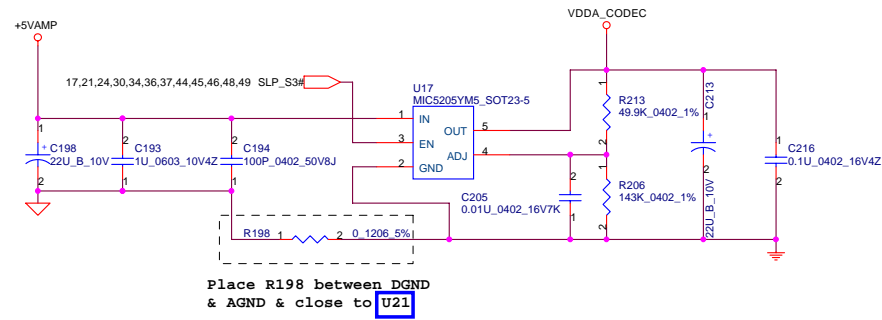
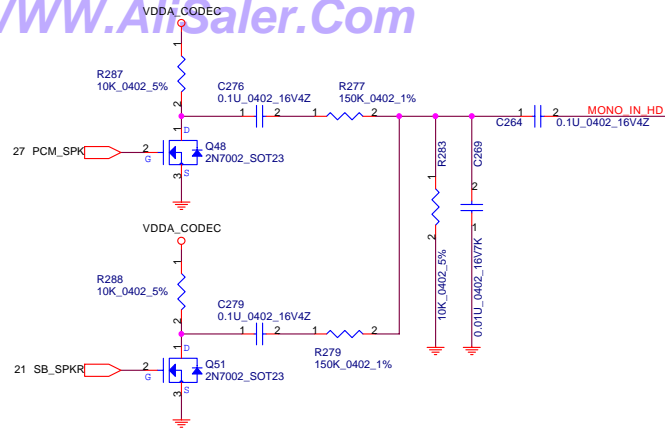
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Issued Date		2005/03/10	Deciphered Date		2006/03/10	Title
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						Size
Date:				星期五, 十一月 10, 2006		Sheet 26 of 55



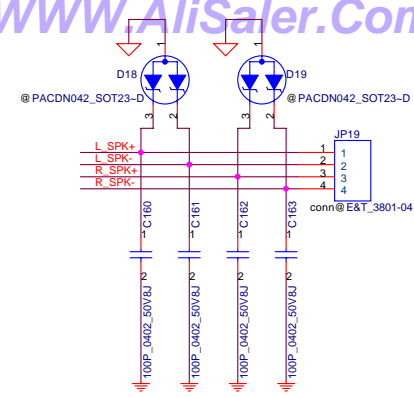
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Issued Date	2006/02/06	Deciphered Date	2007/02/06	Title		
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				Custom	LA-333IP	0.4
				Date:	星期四, 十一月 10, 2006	Sheet 27 of 55



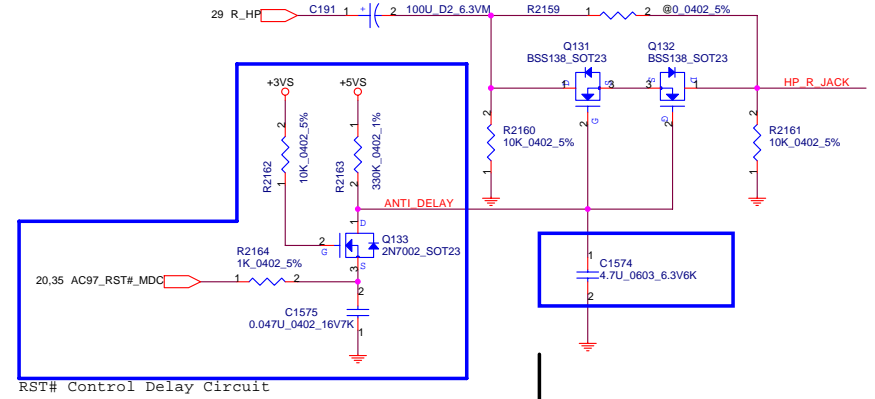
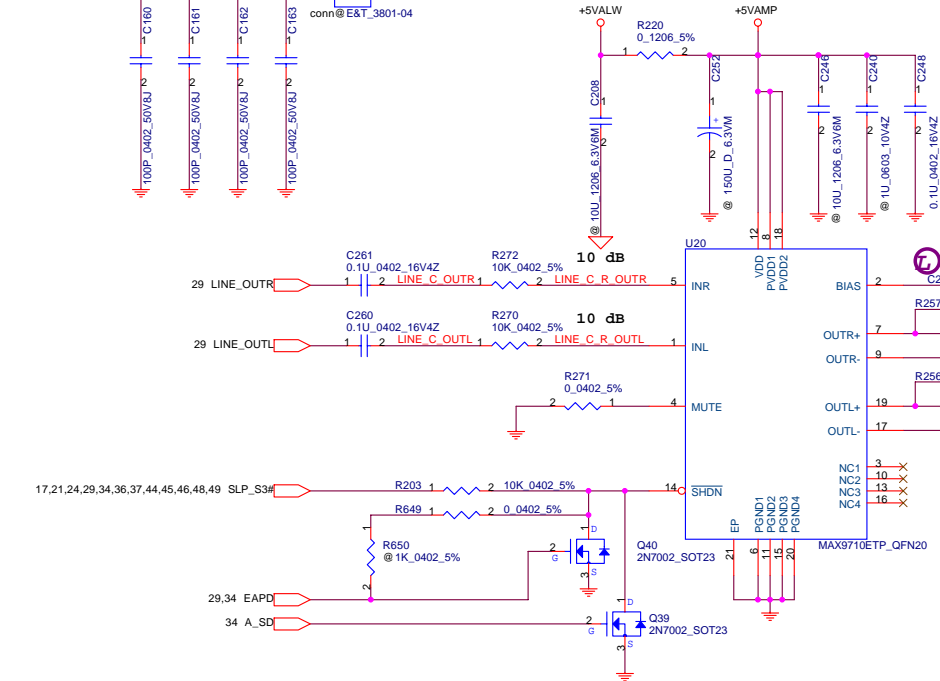
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				Custom	LA-331P	0.4
				Date:	星期二, 二月 10, 2006	Sheet 28 of 55



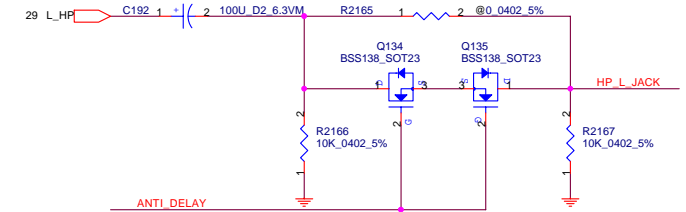
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Issued Date		2005/03/10	Deciphered Date	2006/03/10	Title	
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		Size	Document Number	Rev		
		LA-333IP	0.4			
		Date:	星期日, 十一月 10, 2006	Sheet 29 of 55		



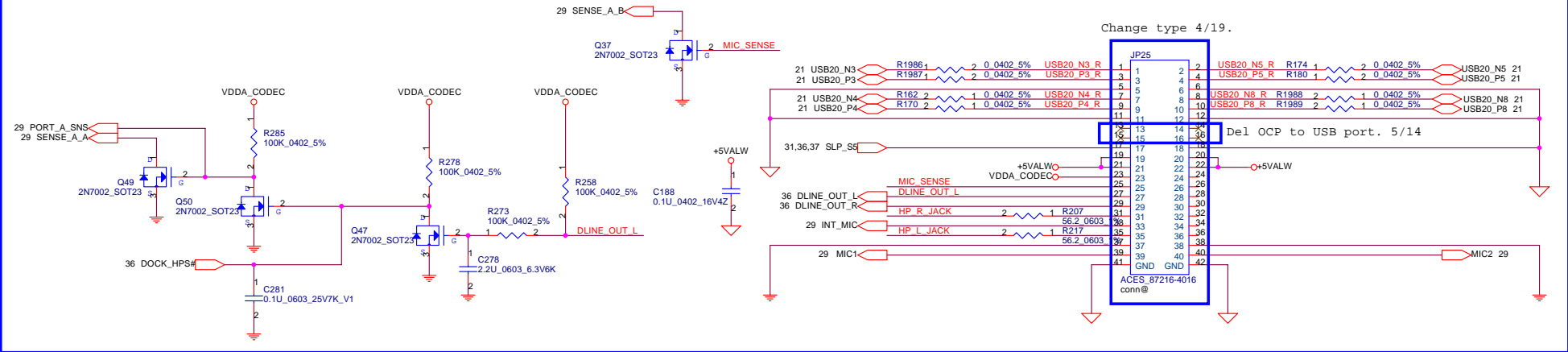
## AMP. FOR INTERNAL SPEAKER



## ANTI POP Circuit (Add in 7/26)



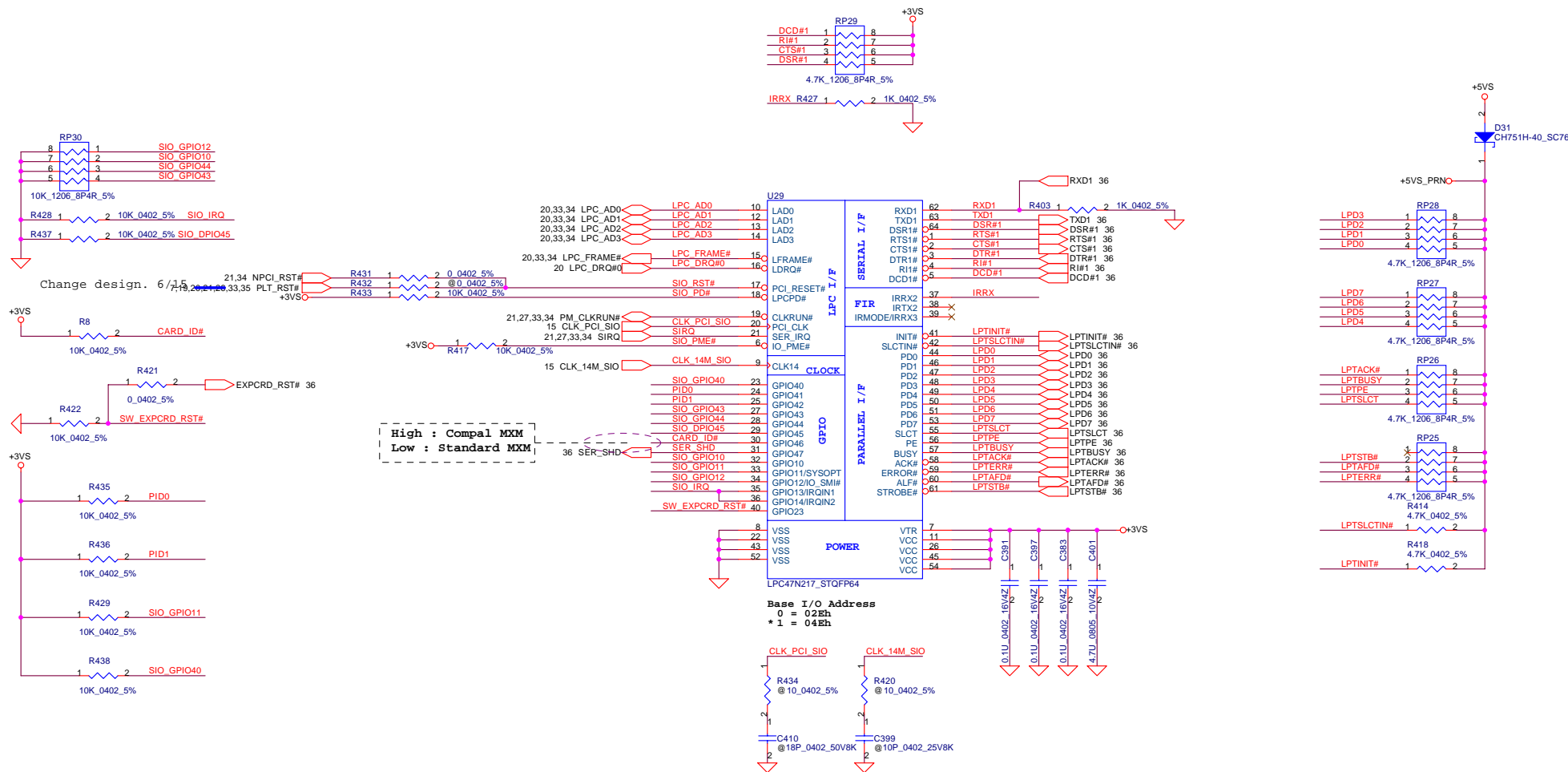
## To Audio / USB Board CONN

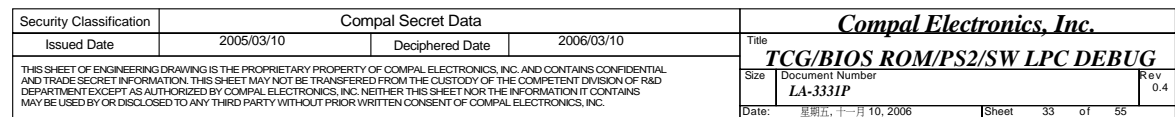


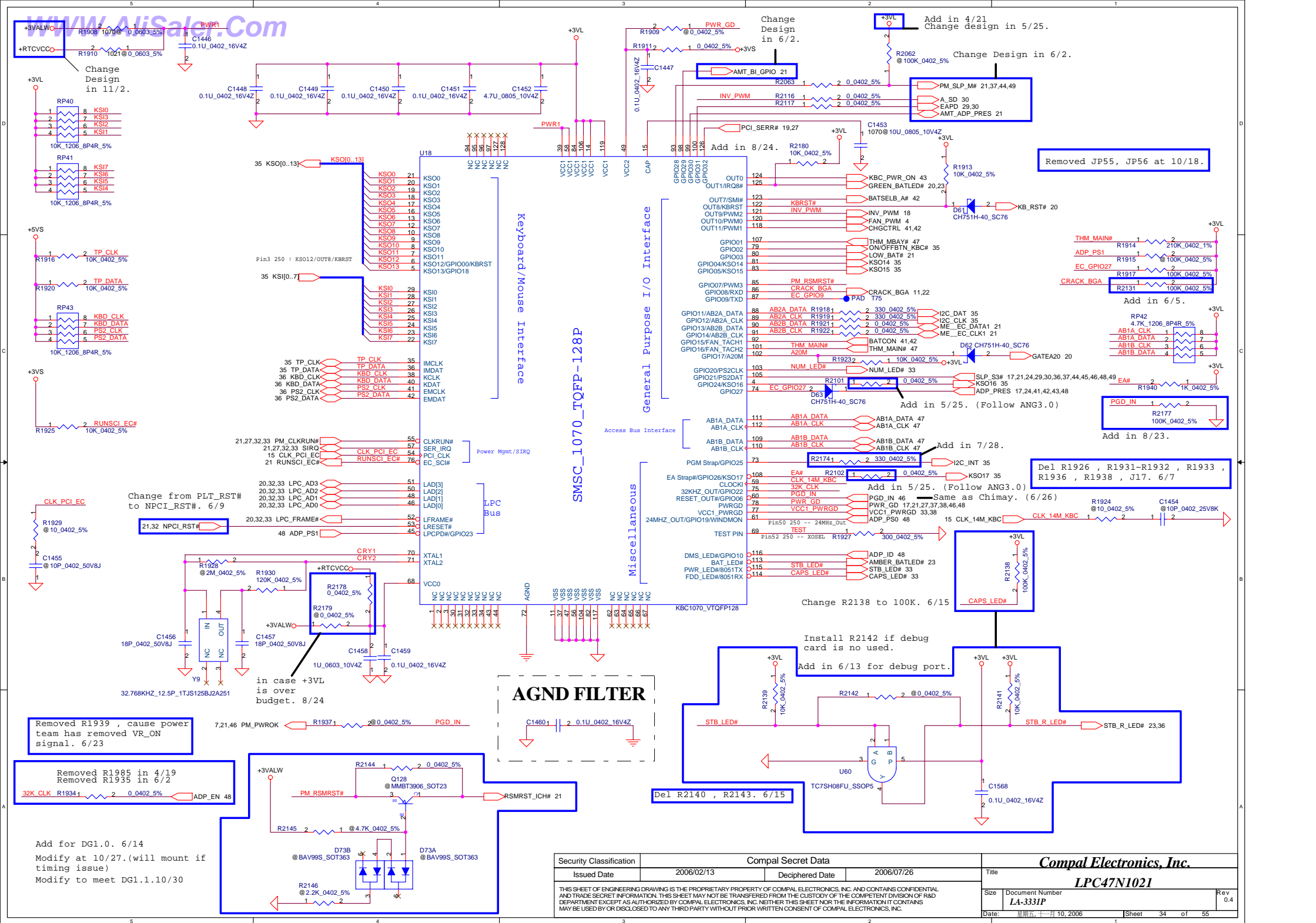
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				LA-333IP	Rev 0.4
Date: 2006/11/10		Sheet 30 of 55		Rev 0.4	

## A

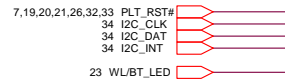




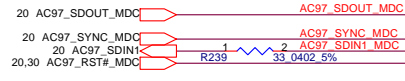




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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title		
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				Size	Document Number	Rev
					LA-3331P	0.4
Date: 星期日, 十一月 10, 2006				Sheet	34	of 55

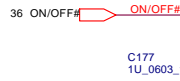


**MDC 1.5 Conn.**



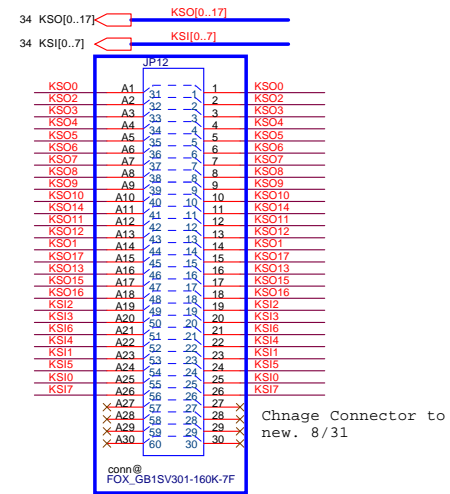
```
Del Modem disable
function(Del
R2147). 6/21.
```

## Power button

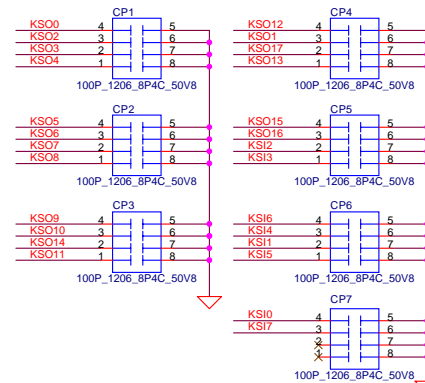


Change to single gate. 5/9

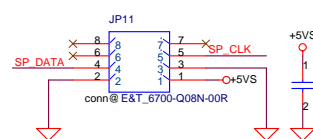
## INT\_KBD\_CONN.



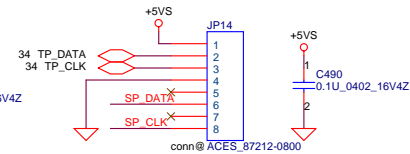
Update to 18x8 angelfire keyboard matrix



## TrackPoint CONN.



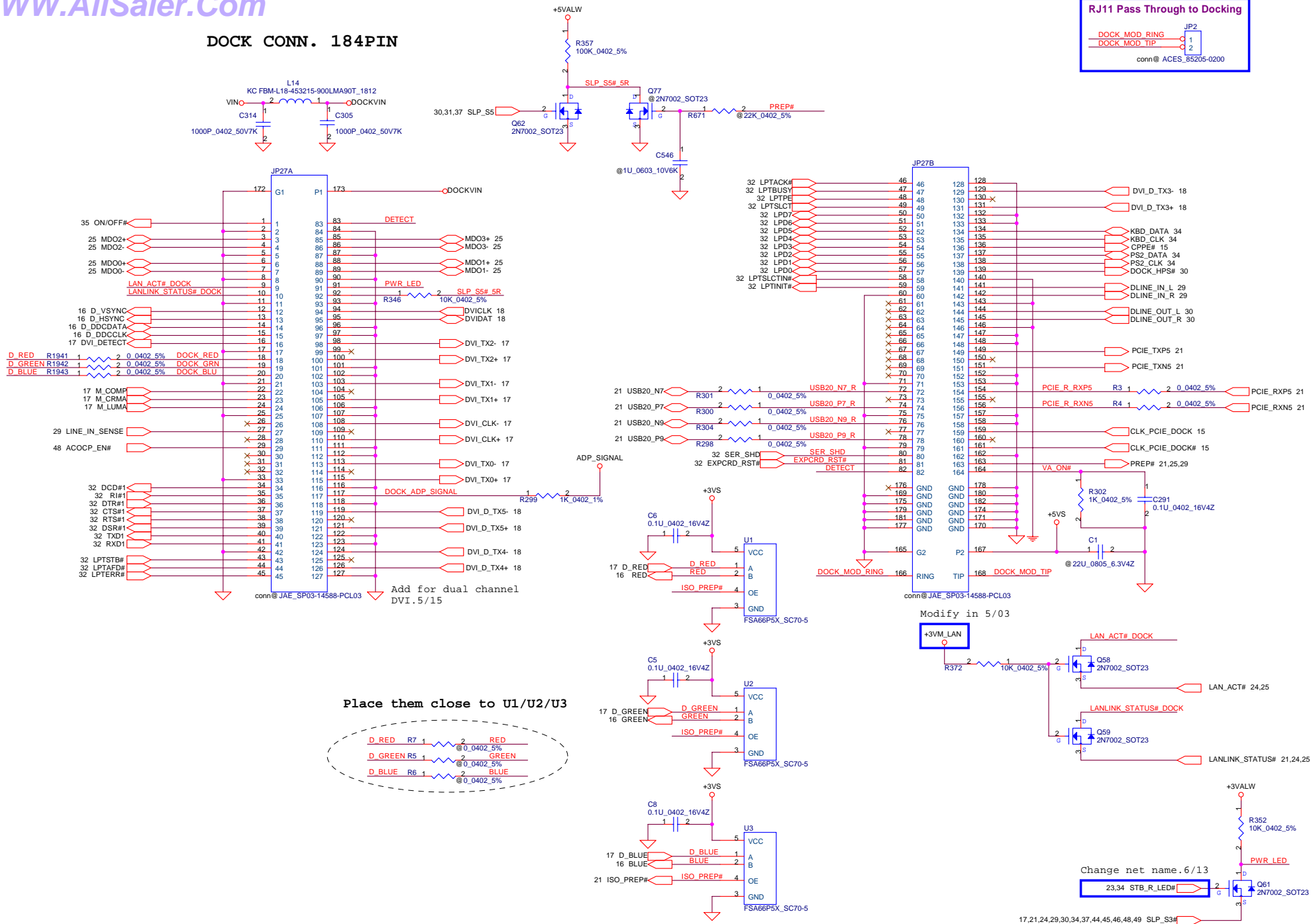
**T/P BOARD.**



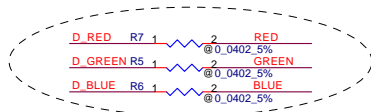
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	<b>MDC/KBD/ON OFF/LID</b>	
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# DOCK CONN. 184PIN

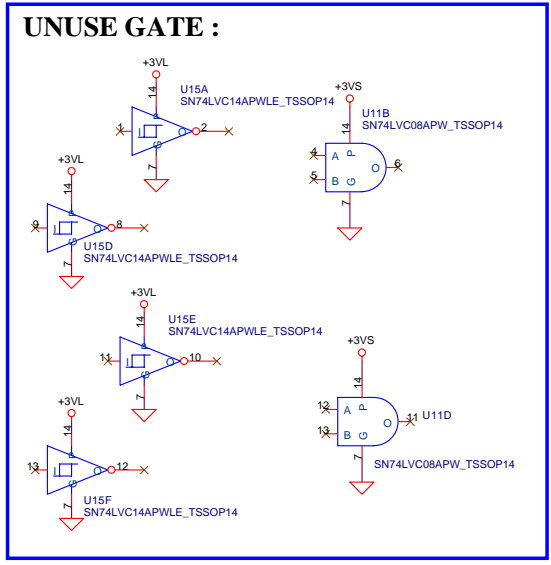
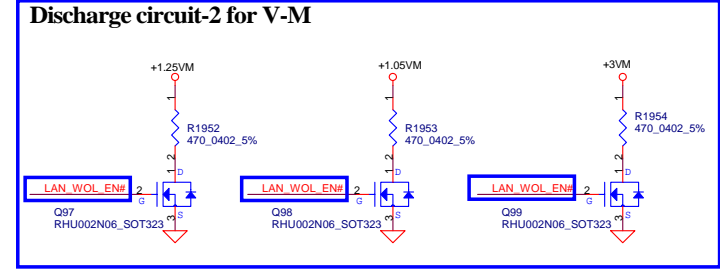
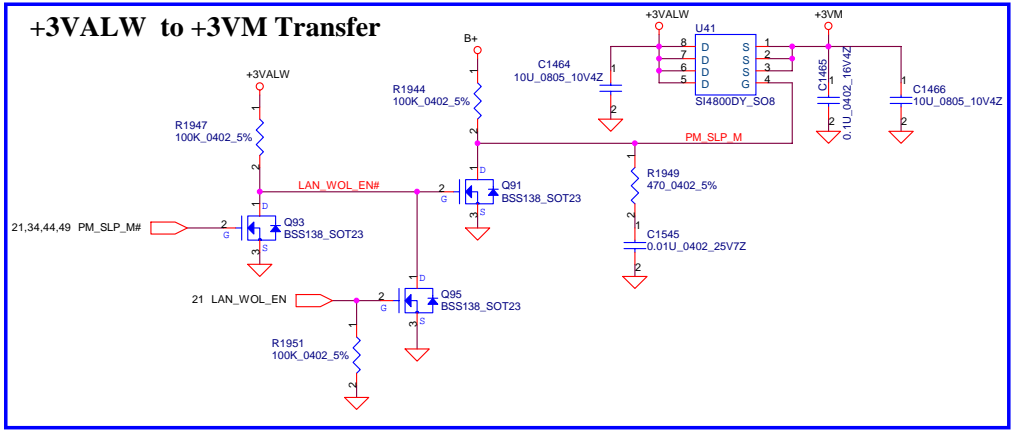
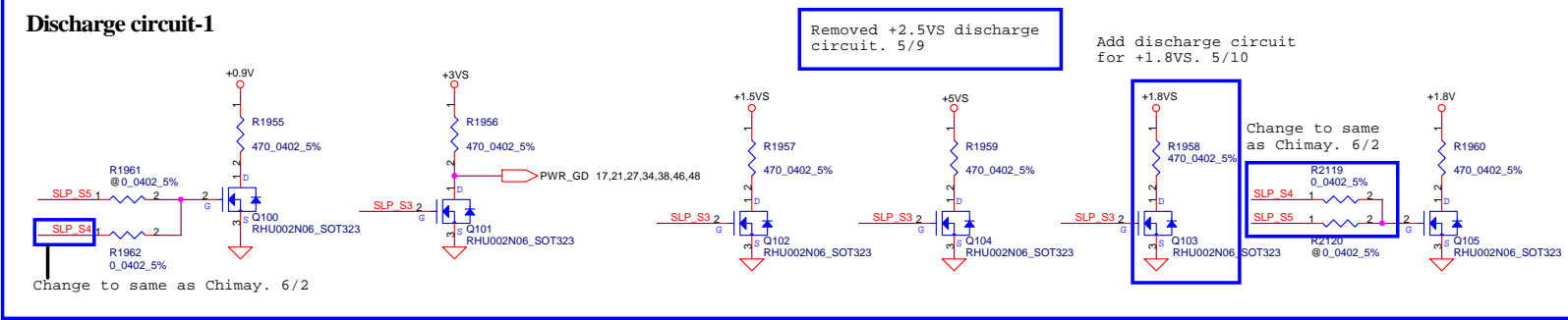
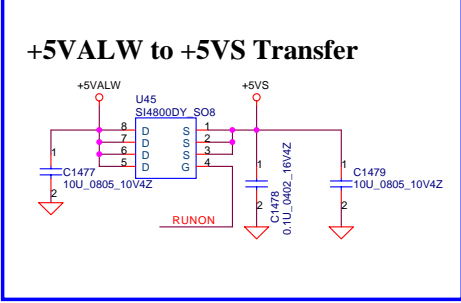
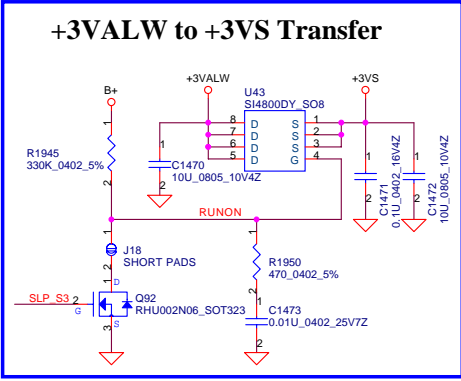
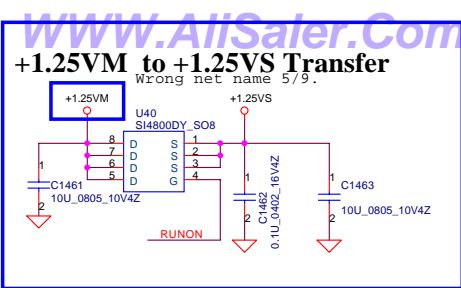
## RJ11 Pass Through to Docking



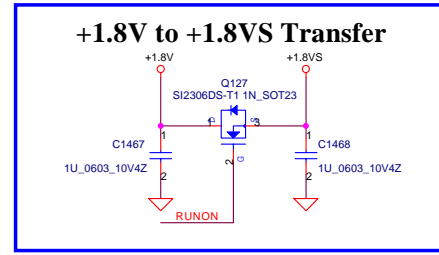
Place them close to U1/U2/U3



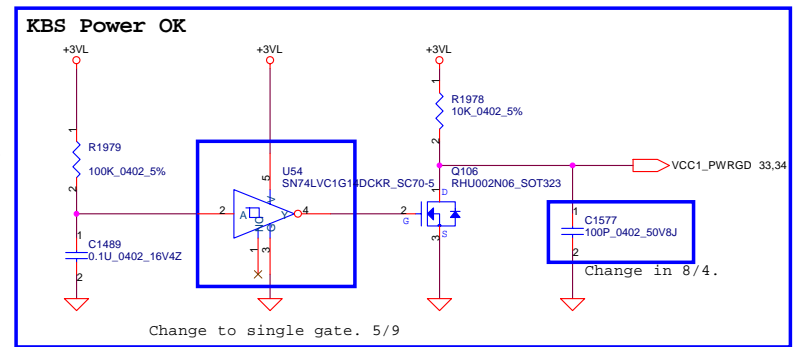
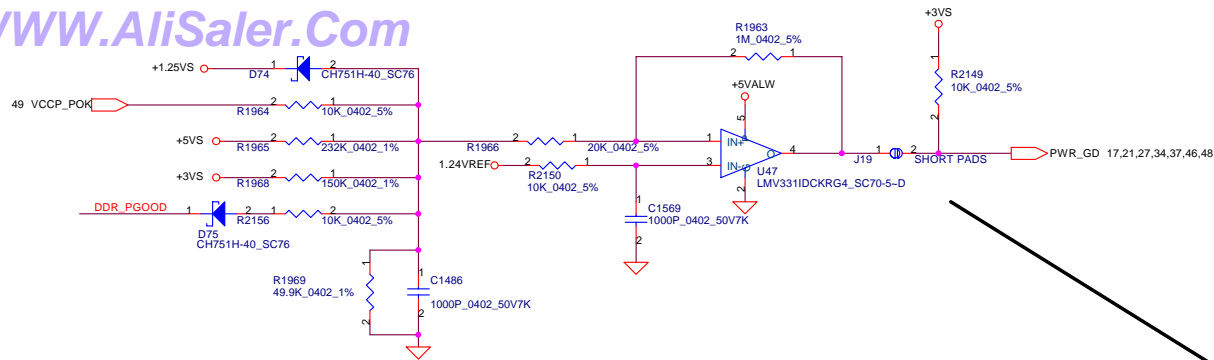
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				LA-333IP	Rev 0.4
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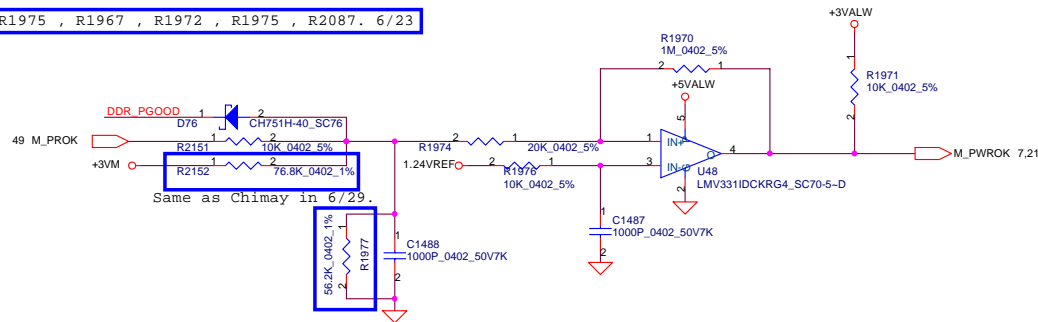
Change U42 to Q , cause no need such power consumption of +1.8VS. 6/9



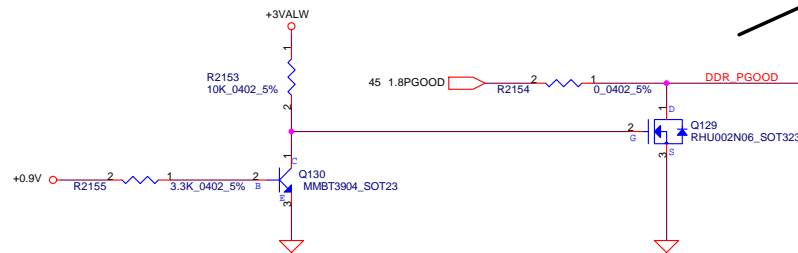
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/07/26	DC/DC Circuits	
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				LA-333IP	Rev 0.4
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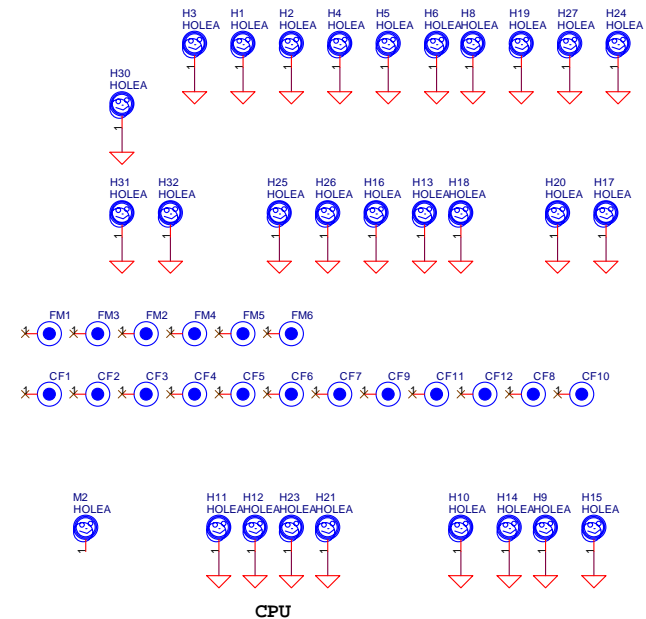
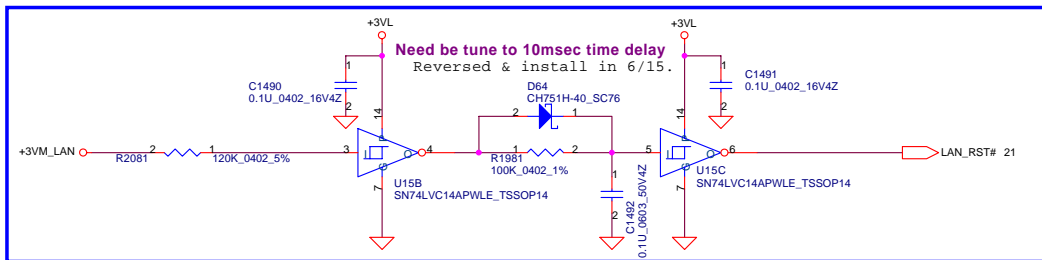
Del R1975, R1967, R1972, R1975, R2087. 6/23



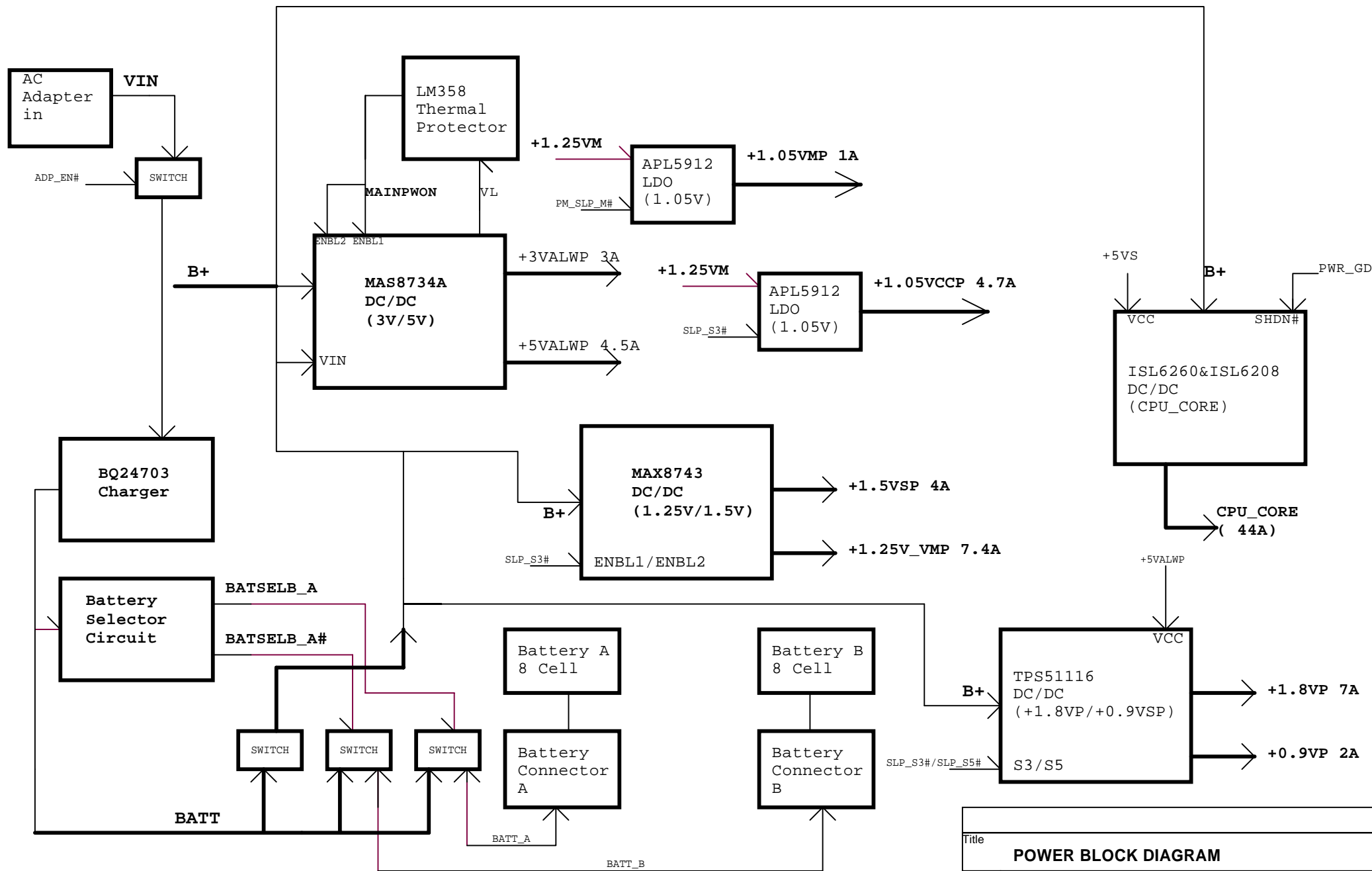
Modify Power good circuit to same as Chimay. 6/23



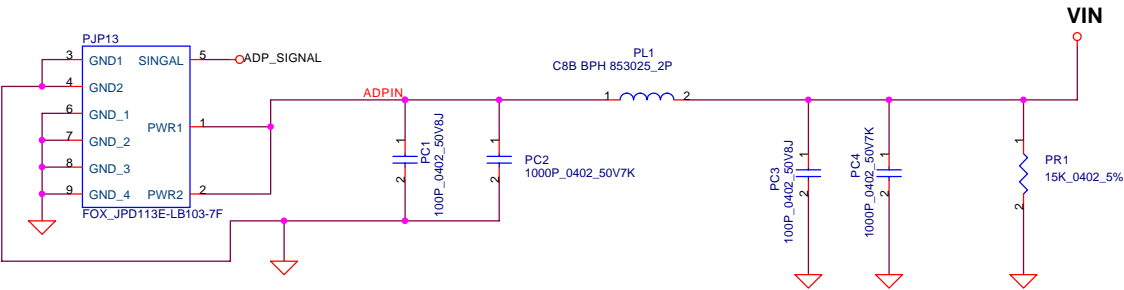
Change to same as Chimay (Del R2080, R1980, R2082. 6/23)  
Modify to same as Chimay 5/5



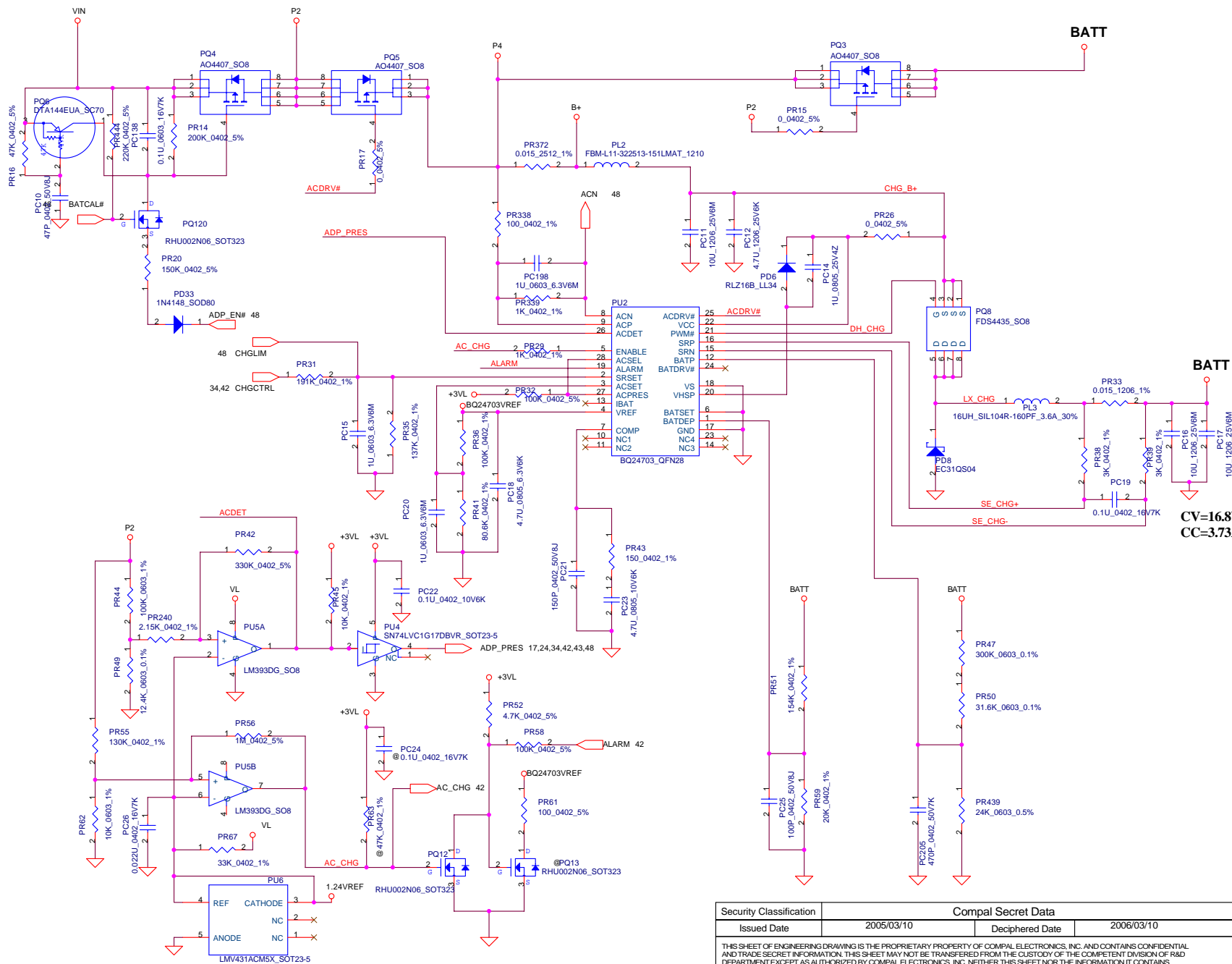
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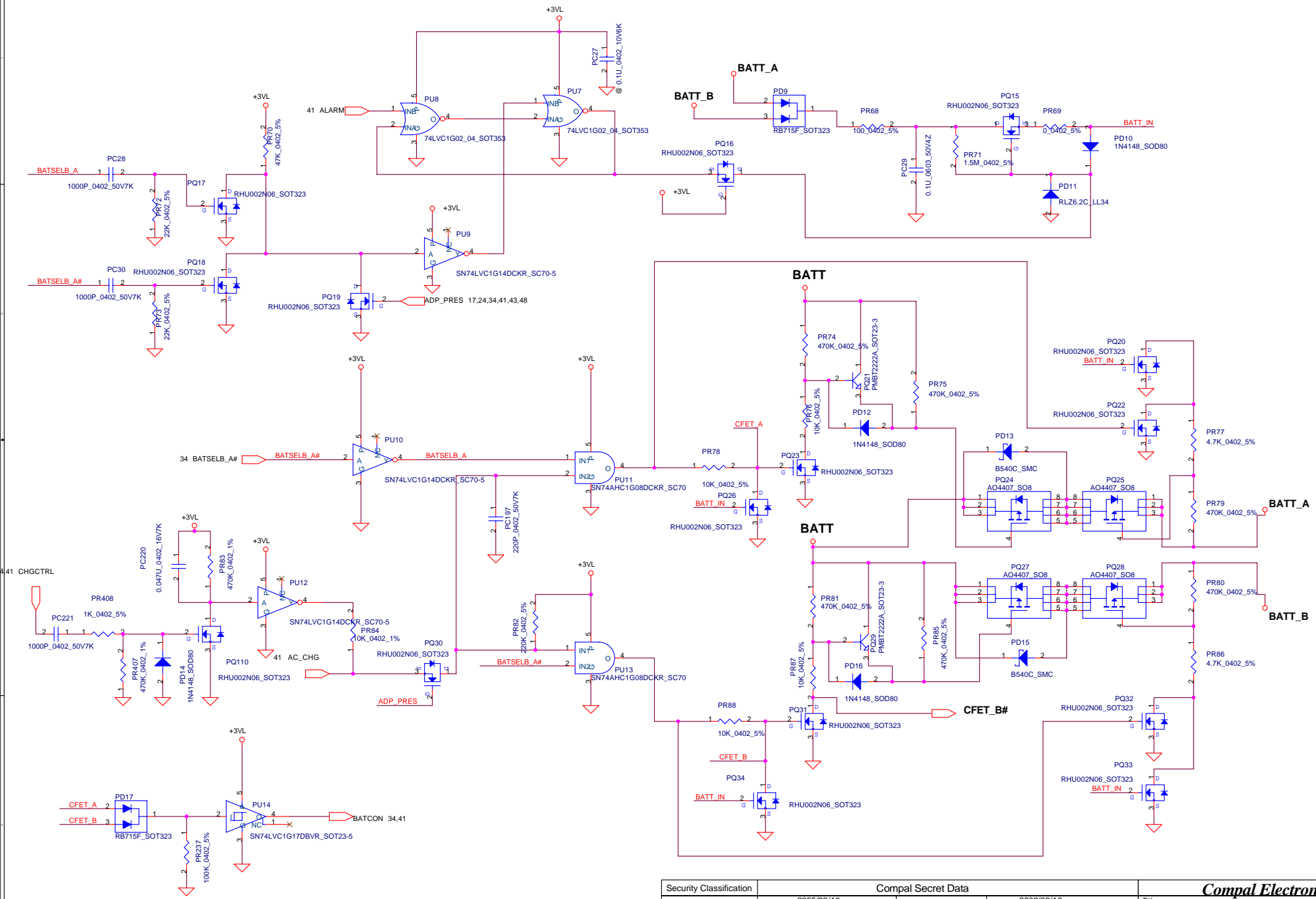
Title		
POWER BLOCK DIAGRAM		
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				Custom	LA-3331P
Date: 星期五, 十一月 10, 2006				Sheet	40 of 55



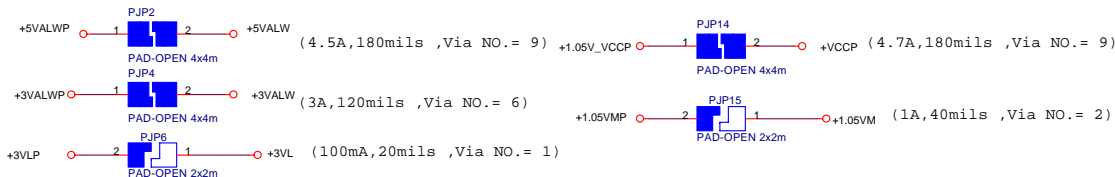
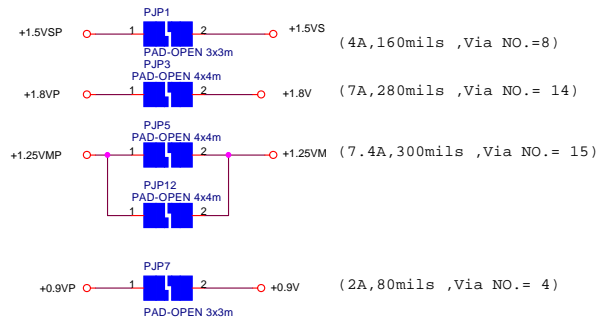
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						Size		Document Number		Rev	
						Customer		LA-3331P			
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Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Compal Electronics, Inc.	
2005/03/10		2006/03/10		Battery selector	
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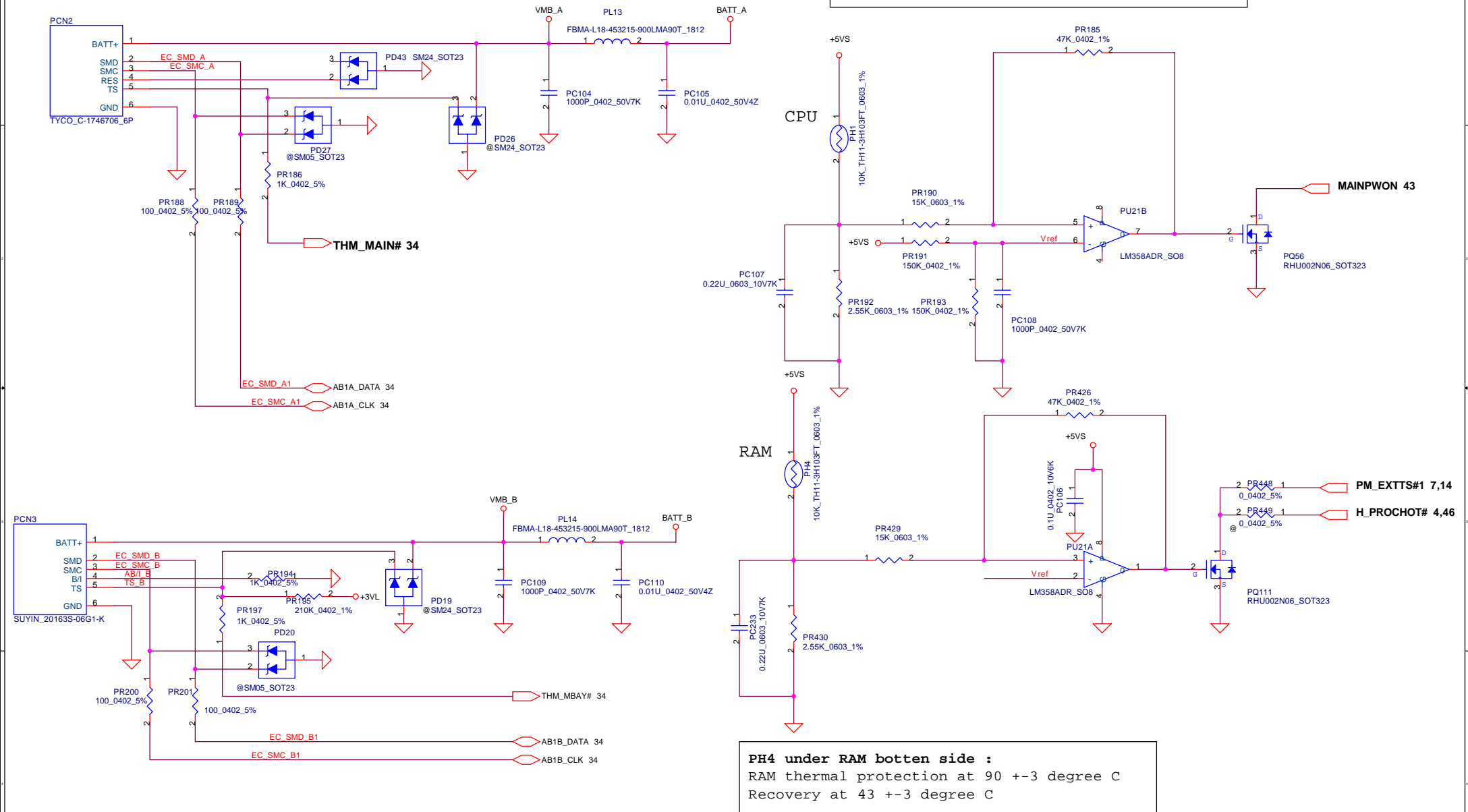




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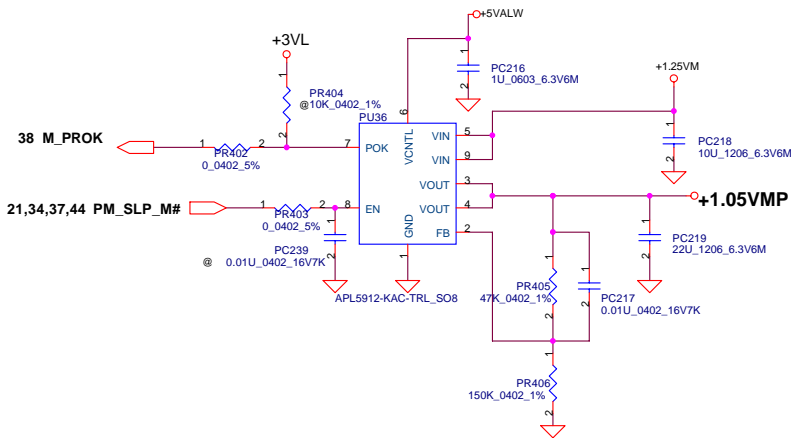
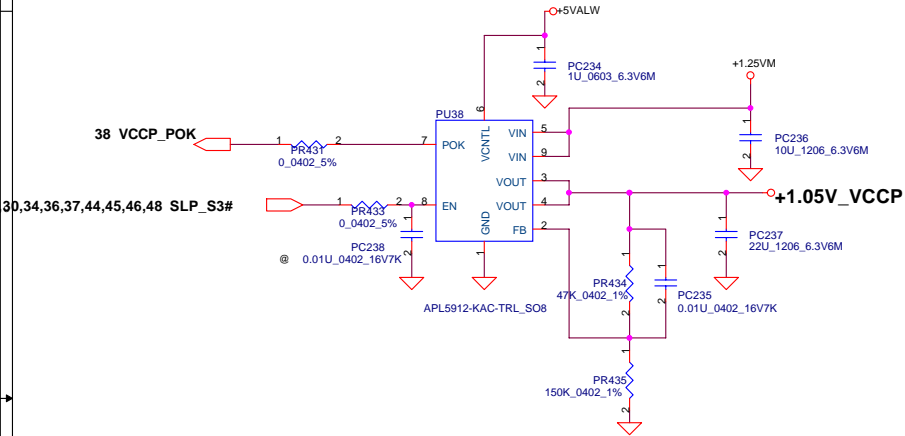






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# Version Change List ( P. I. R, List ) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																																	
1	41	Charger	5/9	HP	Remove PQ91,PD32,PR376	Remove PQ91,PD32,PR376	Rev.																																	
2	42	Battery Selector	5/9	HP	Modify battery selector design.	PU12 Change from SN74LVC1G17DBVR_SOT23-5 to SN74LVC1G14DCKR_SC70-5 Add new location PC220 as 0.047uF Add new location PC221 as 1000PF Add new location PR407 as 470K ohm. Add new location PR408 as 1K ohm.																																		
3	43	3.3VALW/5VALW	5/9	HP	Modify 3.3VALW/5VALW solution	Change solution from TPS51020 to MAX8734A																																		
4	44	2.5VALW/1.5VS/ 1.05VCCP	5/9	Compal	Remove 2.5VALW, H/W no need!	Remove PU20, PC72, PC73																																		
5	47	BATTERY CONN	5/9	Compal Thermal team	Add RAM thermal protection schematic.	Add new location PH4,PC233,PR430,PR429,PR426,PQ111																																		
6	48	ADP_OCP	5/9	HP	Modify ADP_OCP design	Delete PR379,PQ103,PQ104,PR386,PR382,PQ106																																		
7	43	3.3VALW/5VALW	5/9	Compal	Modify 3.3VALW/5VALW location for layout.	Swap location PC33, PC44 Swap location PC34, PC45 Swap location PQ37, PQ38, PL5 PL6, PR100, PR104, PC39 , PC199.																																		
8	44	1.25VM/1.5VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution																																		
9	49	1.05V_VCCP/ 1.05VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution.																																		
10	45	1.8V/0.9VS	6/2	HP	HP request to follow Chimay.	Modify 1.8V/0.9VS schematic.																																		
11	41	Charger	6/6	HP	HP request!	Modify Charger schematic.																																		
12	42	Battery selector	6/6	HP	HP request!	Modify selector schematic.																																		
13	47	BATTERY CONN	6/6	HP	HP request!	Modify main battery power in schematic.																																		
14	45	1.8V/0.9VS	6/7	HP	At S3 mode, 0.9V need exist, so connect PR242 to 1.8V	Modify PR242 connect to 1.8V																																		
15	46	CPU_CORE	6/21	HP	HP request.	Modify PU31.35 pin connect to SLP_S3#, originally is connect to VR_ON.																																		
						<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2006/02/28</td><td>Deciphered Date</td><td>2007/02/28</td><td colspan="2">Title</td></tr><tr><td colspan="4" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td colspan="2">Changed-List History-1</td></tr><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td colspan="4"></td><td>LA-3031P</td><td>0.5</td></tr><tr><td colspan="4">Date: 星期二, 十一月 10, 2006</td><td>Sheet 50 of 55</td><td></td></tr></table>	Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2006/02/28	Deciphered Date	2007/02/28	Title		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Changed-List History-1		Size	Document Number	Rev					LA-3031P	0.5	Date: 星期二, 十一月 10, 2006				Sheet 50 of 55		
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Version Change List ( P. I. R. List ) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Charger	5/9	HP	Change PQ114 to BSS138.	Change PQ114 to BSS138.	
2	47	BATTERY CONN	9/7	Compal	Intel Document for the DDR Module Thermal Diode design	Change the PQ111.1 connection from H_PROCHOT# to PM_EXTTS#1	
3	43/44		11/1	Compal	Dual N MOSFET has failure rate at other project, to reduce Dual N MOS useage.	Change 3V, 1.5V solution, to single N Mos FET solution.	

# Version Change List (P. I. R. List )for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	26	Mini Express Card	7/3	Compal	H28 & H29 size different.	Change H28 size to same as H29.	0.2
2	24	GIGA LAN	7/4	Compal	BOM Leverage to Chimay.	Chnage Y8 to 25MHz_20P_1BG25000CK1A (Same as Chimay)	0.2
3	18	GPIO Extender	7/4	Compal	Use wrong package with BOM (U59).	Correct the package.	0.2
4	34	Capacitive I2C	7/27	HP		Change R1918, R1919 & add R2174 to 330 ohm.	0.2
5	15	FSB SEL	7/27	HP	No good for layout quality.	Del R1719, R1726.	0.2
6	20	RTC Conn	7/26	Compal	Wrong Package	Change JP28 from SP02000D000 to SP02000D700.	0.2
7	33	NUM_LED#	7/25	Compal	System auto re-boot	Add R2168 pull up to 3V <sub>L</sub> .	0.2
8	30	Head Phone	7/26	HP	ANTI-POP noise	Add circuit for this issue	0.2
9	26	WLAN	7/27	HP		Add R2158 connect to +3V <sub>S</sub> and connect to JP30 pin 2,39,41,52 , pin37,43 connect to GND.	0.2
10	18	Quick Switch	7/26	Compal	Wrong package for PCB foot print (U57).	Correct the package.	0.2
11	21	CPU Clock	7/28	Compal/HP	VRMPWRGD has glitch to cause wrong CPU clk.	Add R2173 & reserve C1576.	0.2
12	18	Quick Switch	7/28	Compal	Channel A & B will twist together as current layout.	Swap Channel A & B on schematic.	0.2
13	06	VCCP	8/1	Compal		Delete C1570 ~ C1573	0.2
14	21	CL_VREF1_ICH	8/2	Compal	Wrong pull high to +3VM.(R1855)	Change pull up to +3VALW.	0.2
15	31	USB	8/2	Compal	No pull up resistor for USB power switch OC pin.	Add R2175 and pull up to +5VALW.	0.2
16	18	Quick Switch	8/3	HP		Add U61 and Reserved R2176 for Q-switch select pin.	0.2
17	38	Power Good	8/4	Compal	VCC1_PWRGD has glitch when power on.	Reserve C1577 on PWRGD to GND.	0.2
18	21	Power Good	8/7	Compal	CLK_ENABLE# has glitch when power on.	Change R1862 from 330ohm to 1K ohm.	0.2
19	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
20	27	CardBus Controller	8/15.	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3

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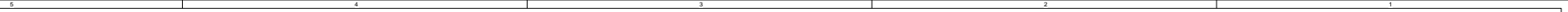
# Version Change List (P. I. R. List )for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
2	27	CardBus Controller	8/15	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3
3	21	USB	8/23	Compal	System easy hang-up when plug USB2.0 device.	Separate from pull up resistor of U10 for these pins.	0.3
4	34	PGD_IN	8/23	HP	Leverage Chimay SI schematic.	Add R2177(100K) pull down to GND.	0.3
5	34	EC VCC0(PIN 68)	8/24	HP	+3VL may over budget.	Add R2178, R2179(RV) for option the power source.	0.3
6	34	EC	8/24	HP	Leverage Chimay SI schematic.	Add D77, R2180 and connect D77 pin2 to U10 pinAE10.	0.3
7	33	SPI ROM	8/24	HP	Debug card asserts hold, can't assert both SPI ROM.	Add R2181 to connect SPI_HOLD#0 and SPI_HOLD#1.	0.3
8	26	MINI Card	8/24	HP	May leakage issue from WLAN card.	Add D78 to prevent this issue.	0.3
9	21	Power Sequency	8/24	HP	There is a shoot when power on of this pin.	Reserve R1862 and add R2182(10K) pull up to PWR_GD.	0.3
10	21	GPIO26	8/24	HP	Default is input can't floating.	Add a pull up R2183(10K) to +3VS.	0.3
11	21	GPIO17	8/24	HP	Default is input can't floating.	Make R2115 from RV to mount.	0.3
12	21	STP_CPU#	8/24	HP	Can't into C3 status.	Mount R1829.	0.3
13	21	XDP_DBRESET#	8/24	HP	Leverage Chimay SI schematic.	Change R1847 to 1K.	0.3
14	21	SPI_CS1#	8/24	HP	Only need one 4MB BIOS chip.	Add R2184(0 ohm) for BOM option.	0.3
15	17	MXM-HE	8/24	HP	Need High performace VGA card.	Chnage MXM-III to MXM-HE.	0.3
16	17	HDMI	8/25	HP	BOM change.	Change R1990 to 1K, R1991 to 10K and add L23, C1578.	0.3
17	21	GPIO12	8/28	HP	Add BOM option for SPI_CS1#.	Change connect of R1845.2 from LAN_PHYPC to LAN_PHYPC_R.	0.3
18	21	GPIO1 & GPIO11	8/28	HP	Net Change.	Exchnage OCP#(To GPIO1)&LANLINK_STATUS#(To GPIO11)	0.3
19	28	Card bus ETD test	8/31	HP	May some issue with ETD test.	Reserved C1509.	0.3
20	35	KBD Connector	8/31	HP	To meet HP 2007 platform defined.	Chnage JP12 from 26pin to 30pin.	0.3
21	10	L22	9/6	HP	BLM18PG221SN1 impedance is 221ohm@100MHz.	BLM18PG330SN1 impedance is 33ohm@100MHz.	0.3
22	26	Wireless LAN	9/6	HP	Connect C217, C171, C493 to wrong power.	Connect C217, C171, C493 from +3VS to +3VS_WLAN.	0.3
23	07	CRESTLINE	9/6	HP	Change Chip version from A0 to B0.	Mount R2134.	0.3
24	04, 21	Second FAN	9/7	Compal	Thermal team ask to add control for second FAN.	Add R2185, R2186 and use GPIO20 to control FAN.	0.3
25	17	MXM power B+	9/8	Compal	Delete C9 cause not enough space to placement.	ADD C1579, C1580(1210 size) to replace C9.	0.3
26	24	LAN Connector	9/12	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	ADD C1581, C1582(0402 size) per EMI request.	0.3

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1	20, 34	BATTERY LED	10/2	HP	GREEN_BATLED# keep high when AC/DC exist.	Change connection between SB & EC.	0.4
2	21	SM Bus	10/3	Compal	SM Bus connection is not correct.	Correct connection of SM bus and reserved R1817, R1820.	0.4
3	35	Function Connector	10/5	HP	Wireless LED always on.	Make change of JP1, pin1-> +3VL, pin2 -> +3VS.	0.4
4	20, 23	Kensington support	10/18	HP	Removed Kensington support.	Remove JP60, Q122, R2084.	0.4
5	18	Quick-Switch	10/18	Nvidia	We will change Quick switch to PI3HDMI412FT-A	Don't need pull up, removed RP44 ~ RP47.	0.4
6	18	Quick-Switch	10/18	HP	Don't have decoupling for U57 1.5VS.	Add C1583, C1584.	0.4
7	34	KBC Debug port	10/18	HP	Don't need use JP55, JP56 for debug.	Removed JP55, JP56 from SI1.	0.4
8	34	RUMRST# timing	10/18	HP	It may don't need these circuit.	Reserve them at SI1.(Install R2144, RV: Q128, D73, R2145~2146)	0.4
9	34	RUMRST# timing	10/18	HP	It different to desgn guide 1.1.	Change R2145 to 4.7k, pull up to +3VALW and connect to Q128 base pin.	0.4
10	34	VCC1 Power	11/02	HP	Chnage Design.	Chnage VCC1 power option to +3VALW or +RTCVCC.	0.4
11	21	LANSTATUS#	11/02	HP	System auto power on after plug AC in.	Add Q136 to isolation U10 directly link to NIC, and add PU R2187.	0.4
12	31	USB Switch	11/03	Compal	Don't need dual layout for USB power switch.	Remove U7, U36.	0.4
13	30	Audio	11/03	HP	To pass Vista test of Audio.	Change R207, R217 from 15ohm to 56.2ohm.	0.4
14	25	LAN	11/06	Intel	Intel Santa Rosa Platform Message of the WW44	Change R1903 from 3.92Kohm to 1.4Kohm.	0.4
15	24	LAN Connector	11/06	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	Mount C1581, C1582 --> 680pF(0402).	0.4
16	17	MXM Connector	11/08	HP	Need BOM option of SLP_S3# for use G71 or G84.	Add R2190(0ohm).	0.4
17	4	Thermal Senser	11/08	HP	Abita will chnage to new Thermal senser in the future.	Add R2188, R2189(0ohm).	0.4
18	35	MDC	11/08	HP	Implement new MDC future.	Connect JP26.2 to +3VS.	0.4
19	15	FSB Freq Selecter	11/09	HP	Need HW option for 667MHz or 800MHz	Add JP62, JP63 and install R1689,R1696,R1705,R1737 and reserve R1694,R1716,R1734.	0.4
20							
21	37	M-Power discharge	11/10	Compal	It's wrong connection of discharge control circuit.	Correct Q97, Q98, Q99 pin2 connect to LAN_WOL_EN#.	0.4
22							
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25							
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